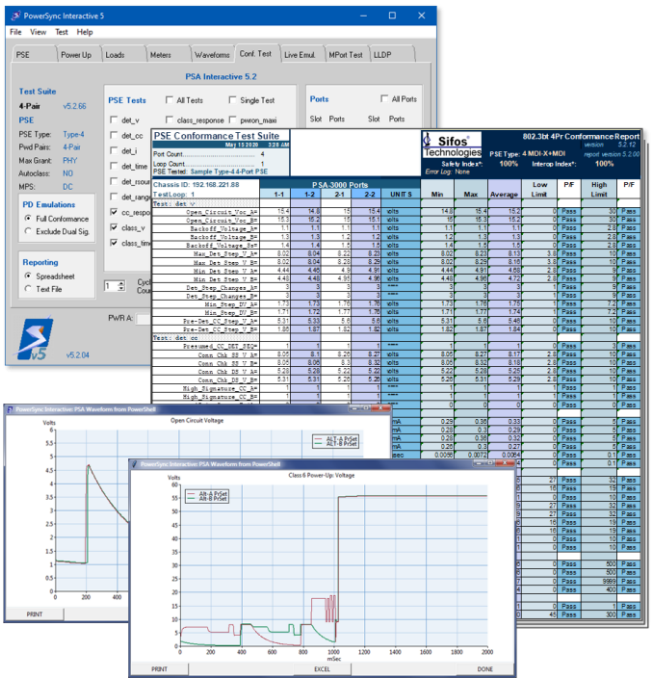
PSA-CT4P

PSE Conformance Test Suite

for 4-Pair 802.3bt PSE's

Product Overview



Key Features

- ❑ **Robust 802.3bt 4-Pair PSE Conformance Testing**
- ❑ **Fully Automated Port Sequencing and Statistics covering up to 24 PSE Ports with one PSA-3000**
- ❑ **Greater than 92% 802.3bt PICS Coverage from 24 Tests Producing up to 344 Test Parameters per Port**
- ❑ **Fully Emulates All Type-1, 2, 3, and 4 PD's Including Single and Dual Signature Classes and PoE LLDP*-Capable PD's**
- ❑ **Test Type-3 and Type-4 PSE's that Allocate Power Using Multi-Event Classification with LLDP* Refinement**
- ❑ **Automatically Adapts to All Prevalent PSE Signaling and Power Management Behaviors**
- ❑ **Configurable Waveform Trace Diagnostic Generation and Retention**
- ❑ **Colorful and Informative Spreadsheet Reporting** with Compliance (Pass/Fail) Notations and Parameter Statistics**
- ❑ **Run & Sequence from PSA Interactive GUI or PowerShell PSA Command Line**

Verification, *Simplified.*

IEEE 802.3 PSE's

4-Pair End Span PSE's

4-Pair Mid-Span PSE's

4-Pair Power Injectors

The Industry "Norm"

Unmatched 802.3bt Specification Coverage

Widely Used by PSE Silicon Manufacturers

Supports EA Gen2 PoE Logo Certification

Fully Automated One-Button Testing

Automatic Adaptation to PSE Probing and PD Qualification Methods

Flexibly Sequence Tests and Test Ports

Pop-Up Spreadsheet Reporting with Statistics and Limit Evaluation

Always Up-To-Date

Constantly Enhanced and Improved

Tracking Service Support Agreement

Responsive Technical Support

* *LLDP Emulation & Analysis feature license is sold separately.*
** *Microsoft Excel 2007 or later required*

Overview

With the introduction of the IEEE 802.3bt standard, Power-over-Ethernet expanded from a 30W powering system to a 90W powering system that utilizes all four wire pairs within Cat 5/6/7 cabling. In order to facilitate this change, extensive new features were added placing many new demands on both power sourcing equipment (PSE's) and powered devices (PD's). On the PSE side, the added complexity is perhaps best demonstrated by the IEEE 802.3 state machine growth from 4 pages in 802.3at to 31 pages in802.3bt.

Higher Power, Higher Flexibility with 802.3bt

Before 802.3bt, PD's were restricted to receiving power on two wire pairs with a maximum load at the PD interface of 25.5 watts. With 802.3bt, PD's can be designed to draw over 70 watts from four wire pairs and further, PD's may choose to combine that power to one integrated power load or to split it into two autonomous power loads. PSE's are challenged to recognize 13 different classes of PD's and power those classes appropriately while also overcoming imperfections in cabling and components that cause 4-pair power to divide unevenly between wire pairs. While 802.3at introduced one mode of PD power demotion, 802.3bt introduces 27 possible scenarios whereby PD's are granted less power than requested.

The 802.3bt standard also specifies an enhanced PoE Link Layer Discovery Protocol (LLDP) that includes a number of new TLV's while maintaining PD power allocations with a granularity of 0.1 watt.

Fully Automated Testing with Very High Test Coverage

Given the complexity of a fully compliant 4-Pair 802.3bt PSE, the range of test cases that must be run is so enormous as to prohibit manual testing as a practical solution. The 4-Pair PSE Conformance Test Suite produces over 300 test parameters for each PSE port tested with a maximum possible count of 352 test parameters. The test suite automatically adapts to a wide range of possible PSE implementations and produces a number of implementation-specific test parameters.

The 25 tests that make up the 4-Pair Conformance Test Suite cover **92% of the PSE PICS** in the IEEE 802.3bt including those individual PICS that cover dozens of technical specifications. The 4-Pair PSE Conformance Test Suite is widely used throughout the internetworking community as the industry "norm" for PSE specification compliance.

EA Certified 2.0™

Combined with the PowerSync Analyzer, the 4-Pair PSE Conformance Test Suite is qualified for Ethernet Alliance **Gen2 PoE Logo Certification** testing enabling manufacturers to perform the testing required for EA PoE Logo marks in-house.

IEEE 802.3af, 802.3at, 802.3bt Cross-Compatibility

All 802.3bt PSE's must properly recognize and power PD's developed under the 802.3af, 802.3at, and 802.3bt standards. The 4-Pair PSE Conformance Test Suite includes emulations of many PD's including those conforming to the older standards.

Robust Diagnostics and Reporting

The 4-Pair PSE Conformance Test Suite automatically sequences to a pop-up spreadsheet report with full color notations of parameter pass/fail state per port and cross-port statistics for each parameter. Also included are Sifos proprietary scores for PSE Safety and PSE Interoperability.

Verification, Simplified.

PSE Conformance Tests & Parameters

Detection & Connection Check Probing and Functional Tests

det_v — Detection Probe Physical Parameters

Captures and analyzes PSE detection probe voltages with both valid and slightly non-valid detection signatures emulating single and dual signature PD's.

Open_Circuit_Voc_A	Peak Open Circuit Detection Voltage on Alt-A Pairset
Open_Circuit_Voc_B	Peak Open Circuit Detection Voltage on Alt-B Pairset
Backoff_Voltage_A	IDLE State voltage during detection backoff on the Alt-A Pairset
Backoff_Voltage_B	IDLE State voltage during detection backoff on the Alt-A Pairset
Backoff_Voltage_Ss	IDLE State voltage during Single Signature detection backoff across both Pairsets (as a single signature PD would detect it)
Max_Det_Step_V_A	Maximum Detection Voltage with Valid Detection Signature - Alt-A Pairset
Max_Det_Step_V_B	Maximum Detection Voltage with Valid Detection Signature - Alt-B Pairset
Min_Det_Step_V_A	Minimum Valid Step Voltage with Valid Detection Signature - Alt-A Pairset
Min_Det_Step_V_B	Minimum Valid Step Voltage with Valid Detection Signature - Alt-B Pairset
Det_Step_Changes_A	Count of Detection Step Transitions on the Alt-A Pairset
Det_Step_Changes_B	Count of Detection Step Transitions on the Alt-B Pairset
Min_Step_DV_A	Detection Step Magnitude from Max Voltage to Min Voltage - Alt-A Pairset
Min_Step_DV_B	Detection Step Magnitude from Max Voltage to Min Voltage - Alt-A Pairset
Pre-Det_CC_Step_V_A	Magnitude of any non-802 pre-detection signaling on the Alt-A Pairset
Pre-Det_CC_Step_V_B	Magnitude of any non-802 pre-detection signaling on the Alt-A Pairset

det_cc — Connection Check Probe Physical Parameters

Captures and analyzes PSE 4-pair connection check probe voltages with both valid and slightly non-valid detection signatures emulating single and dual signature PD's.

Presumed_CC_DET_SEQ	CC_DET_SEQ as described by the 802.3bt PSE State Machine, derived from observations of signaling at the PSE physical interface.
Conn_Chk_SS_V_A	Peak connection check voltage on the Alt-A Pairset with Single Signature
Conn_Chk_SS_V_B	Peak connection check voltage on the Alt-B Pairset with Single Signature
Conn_Chk_DS_V_A	Peak connection check voltage on the Alt-A Pairset with Dual Signature
Conn_Chk_DS_V_B	Peak connection check voltage on the Alt-B Pairset with Dual Signature
High_Signature_CC_A	Flag indicating invalid signature compliance to PSE state machine on the Alt-A Pairset. 1 is a PASS, 0 is a FAIL.
High_Signature_CC_B	Flag indicating invalid signature compliance to PSE state machine on the Alt-B Pairset. 1 is a PASS, 0 is a FAIL
4Pair_Start_Fail	Flag indication that the 4-Pair PSE failed to produce any signaling on at least one Pairset when a valid PD signature was connected.

det_i — Detection Current Limiting and Slew Rate

Measures maximum current sourcing capability from a PSE during detection. This behavior is essential to protecting non-PD's connected to the PSE.

Isc_Init_A	Peak detection current @ >1.5V on the Alt-A Pairset
Isc_Init_B	Peak detection current @ >1.5V on the Alt-B Pairset
Isc_Det_A	Peak detection current @ >2.2V on the Alt-A Pairset
Isc_Det_B	Peak detection current @ >2.2V on the Alt-B Pairset
Det_Slew_A	Maximum expected detection voltage slew rate on the Alt-A Pairset
Det_Slew_B	Maximum expected detection voltage slew rate on the Alt-B Pairset

det_time — Detection & Connection Check Timing

Measures detection backoff and detection / connection check probe timing parameters.

Detect_Time_Tdet_A	Time from start of detection until end of detection on the Alt-A Pairset
Detect_Time_Tdet_B	Time from start of detection until end of detection on the Alt-A Pairset

Detection & Connection Check Probing and Functional Tests

Backoff_Time_SS	(IDLE state) Time from end of a detection sequence until start of a new detection sequence given an invalid Single Signature
Det2Det_Time	CC_DET_SEQ 0, 1, and 3 ONLY: The time duration between the end of detection on the PRI Pairset and the start of detection on the SEC pairset.
Det+CC_Time	CC_DET_SEQ 2 ONLY: The total time duration of Detection on both pairsets and Connection Check.
CC2Det_Time	CC_DET_SEQ 0, 3 ONLY: The time from end of Connection Check until start of the first Pairset Detection.

det_rsource — Detection Source Impedance

Determine the type of detection probe (voltage versus current probing) and determine effective source impedance of a current probing scheme. Assesses risk of PSE port powering another PSE port.

PSE_Detect_Source	PSE Detection Scheme. 0= Voltage probing, 1= Current probing.
PSE_Source_Zout_A	The source impedance of the Detection probing on the Alt-A Pairset. A pure voltage source will report as 0 Ω.
PSE_Source_Zout_B	The source impedance of the Detection probing on the Alt-B Pairset. A pure voltage source will report as 0 Ω.

det_range — Detection Accept and Reject Ranges

Assesses the range of acceptable PD signatures given both single and dual signature PD emulations.

Rgood_Max_Single	Maximum Detection signature resistance that gets powered given a Single Signature PD
Rgood_Min_Single	Minimum Detection signature resistance that gets powered given a Single Signature PD
Cgood_Max_Single	Maximum Capacitive signature that gets powered given a Single Signature PD
Rgood_Max_Dual_A	Maximum Detection signature resistance that gets powered on the Alt-A Pairset given a Dual Signature PD
Rgood_Max_Dual_B	Maximum Detection signature resistance that gets powered on the Alt-B Pairset given a Dual Signature PD
Rgood_Min_Dual_A	Minimum Detection signature resistance that gets powered on the Alt-A Pairset given a Dual Signature PD
Rgood_Min_Dual_B	Minimum Detection signature resistance that gets powered on the Alt-B Pairset given a Dual Signature PD
Cgood_Max_Dual_A	Maximum Capacitive signature that gets powered on the Alt-A Pairset given a Dual Signature PD
Cgood_Max_Dual_B	Maximum Capacitive signature that gets powered on the Alt-B Pairset given a Dual Signature PD

cc_response — Connection Check Validity

Determines that connection check performed by a 4-pair PSE properly resolves single versus dual signature PD implementations. Also assesses PSE response to a 2-pair PD connection.

Single_Sig_Response	Flag indicating that the PSE properly characterized a Single Signature PD prior to powering. 1= Success, 0= Failure.
Dual_Sig_Response	Flag indicating that the PSE properly characterized a Dual Signature PD prior to powering. 1= Success, 0= Failure.
2Pair_PD_A	Flag indicating the count of Pairsets powered when a valid PD signature is connected only on the Alt-A Pairset. 0= No Pairsets powered, 1= Alt-A Pairset powered, 2= both pairsets powered.
2Pair_PD_B	Flag indicating the count of Pairsets powered when a valid PD signature is connected only on the Alt-B Pairset. 0= No Pairsets powered, 1= Alt-A Pairset powered, 2= both pairsets powered.

Classification Probing and Functional Tests

class_v — Classification Voltages

Captures and analyzes PSE classification and class probe voltage levels, focusing on only the final classification performed prior to power-up. Also analyzes class probe reset where presented.

Vclass_max_SS	Maximum Class Event Voltage measured as the peak of both pairsets given a Single Signature PD emulation
Vclass_min_SS	Minimum Class Event Voltage measured as the peak of both pairsets given a Single Signature PD emulation

Classification Probing and Functional Tests

Vmark_SS	Median Mark region voltage from the peak of both pairsets given a Single Signature PD emulation
Vreset_SS	If the PSE utilizes a Class Probe given Single Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification. Reports -1 if there is no class reset.
Vclass_max_DSA	Maximum Class Event Voltage on the Alt-A Pairset given a Dual Signature PD emulation
Vclass_max_DSB	Maximum Class Event Voltage on the Alt-B Pairset given a Dual Signature PD emulation
Vclass_min_DSA	Minimum Class Event Voltage on the Alt-A Pairset given a Dual Signature PD emulation
Vclass_min_DSB	Minimum Class Event Voltage on the Alt-B Pairset given a Dual Signature PD emulation
Vmark_DSA	Median Mark region voltage on the Alt-A Pairset given a Dual Signature PD emulation
Vmark_DSB	Median Mark region voltage on the Alt-B Pairset given a Dual Signature PD emulation
Vreset_DSA	If the PSE utilizes a Class Probe given Dual Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification on the Alt-A Pairset. Reports -1 if there is no class reset.
Vreset_DSB	If the PSE utilizes a Class Probe given Dual Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification on the Alt-**A** Pairset. Reports -1 if there is no class reset.

class_time — Classification Timing

Captures and analyzes PSE classification signal timing, focusing on only the final classification performed prior to power-up.

Class_Probe_SS	Flag indicating if a Class Probe is discovered given a Single Signature PD. 1= Class Probe Discovered, 0= No Class Probe.
EV_Count_7_SS	Class Event Count in response to Class 7 (Single Signature) PD on either the Alt-A or Alt-B pairset.
Long_EV1_Time_SS	Duration of Event #1 (LCE) Class Pulse prior to power-up given a Single Signature PD connection.
Min_Class_EV_Time_SS	Minimum duration of any non-LCE Class Event prior to power-up given a Single Signature PD.
Max_Class_EV_Time_SS	Maximum duration of any non-LCE Class Event prior to power-up given a Single Signature PD.
Min_Mark_EV_Lowl_SS	First mark event time duration given a low 0.5mA mark load from PD.
Min_Mark_EV_Time_SS	Minimum duration of any non-final Mark Event prior to power-up given a Single Signature PD.
Max_Mark_EV_Time_SS	Maximum duration of any non-final Mark Event prior to power-up given a Single Signature PD.
Final_Mark_EV_Time_SS	Duration of the final Mark Event leading into Power-Up given a Single Signature PD.
Cl_Prb_Reset_Time_SS	If the PSE utilizes a Class Probe given Single Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1. Set to -1 if no class probing.
Class_Probe_DA	Flag indicating if a Class Probe is discovered on the Alt-A Pairset given a Dual Signature PD. 1= Class Probe Discovered, 0= No Class Probe.
EV_Count_5D_DA	Class Event Count on the Alt-A Pairset in response to a Dual Class 5 PD
Long_EV1_Time_DA	Duration of Event #1 (LCE) Class Pulse prior to power-up on the Alt-A Pairset given a Dual Signature PD connection.
Min_Class_EV_Time_DA	Minimum duration of any non-LCE Class Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.
Max_Class_EV_Time_DA	Maximum duration of any non-LCE Class Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.
Min_Mark_EV_Time_DA	Minimum duration of any non-final Mark Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.
Max_Mark_EV_Time_DA	Maximum duration of any non-final Mark Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.
Final_Mark_EV_Time_DA	Duration of the final Mark Event on the Alt-A Pairset leading into Power-Up given a Dual Signature PD.
Cl_Prb_Reset_Time_DA	If the PSE utilizes a Class Probe on the Alt-A Pairset given a Dual Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1. Set to -1 if no class probing.
Class_Probe_DB	Flag indicating if a Class Probe is discovered on the Alt-B Pairset given a Dual Signature PD. 1= Class Probe Discovered, 0= No Class Probe.
EV_Count_5D_DB	Class Event Count on the Alt-B Pairset in response to a Dual Class 5 PD
Long_EV1_Time_DB	Duration of Event #1 (LCE) Class Pulse prior to power-up on the Alt-B Pairset given a Dual Signature PD connection.
Min_Class_EV_Time_DB	Minimum duration of any non-LCE Class Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.

Classification Probing and Functional Tests

Max_Class_EV_Time_DB	Maximum duration of any non-LCE Class Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.
Min_Mark_EV_Time_DB	Minimum duration of any non-final Mark Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.
Max_Mark_EV_Time_DB	Maximum duration of any non-final Mark Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.
Final_Mark_EV_Time_DB	Duration of the final Mark Event on the Alt-B Pairset leading into Power-Up given a Dual Signature PD.
Cl_Prb_Reset_Time_DB	If the PSE utilizes a Class Probe on the Alt-B Pairset given a Dual Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1. Set to -1 if no class probing.

class_response — PSE Classification Responses to All PD Types

Evaluates PSE responses to a variety of PD types including both single and dual signature. Assesses maximum power PSE will grant at power-up and PSE 2-pair powering behavior.

Class_3_Count	Class Event count in response to Class 3 (Single Signature) PD
Class_4_Count	Class Event count in response to Class 4 (Single Signature) PD
Class_5_Count	Class Event count in response to Class 5 (Single Signature) PD
Class_6_Count	Class Event count in response to Class 6 (Single Signature) PD
Class_7_Count	Class Event count in response to Class 7 (Single Signature) PD
Class_8_Count	Class Event count in response to Class 8 (Single Signature) PD
Class_2D_Count_A	Class Event count on the Alt-A Pairset in response to a Dual Class 2 PD
Class_2D_Count_B	Class Event count on the Alt-B Pairset in response to a Dual Class 2 PD
Class_3D_Count_A	Class Event count on the Alt-A Pairset in response to a Dual Class 3 PD
Class_3D_Count_B	Class Event count on the Alt-B Pairset in response to a Dual Class 3 PD
Class_4D_Count_A	Class Event count on the Alt-A Pairset in response to a Dual Class 4 PD
Class_4D_Count_B	Class Event count on the Alt-B Pairset in response to a Dual Class 4 PD
Class_5D_Count_A	Class Event count on the Alt-A Pairset in response to a Dual Class 5 PD
Class_5D_Count_B	Class Event count on the Alt-B Pairset in response to a Dual Class 5 PD
Max_SS_Class	Maximum Assigned Class available to Single Signature PD's
Max_DS_Class	Maximum Assigned Class available to both pairsets of Dual Signature PD's
Init_Grant_Match	Flag indicating that the maximum power granted to Dual Signature PD's corresponds to the maximum power granted to Single Signature PD's. 1= Correspondance, 0 = Inconsistent
2-Pair_Pairset	Flag indicating which Pairset gets 2-Pair powered if and when the PSE performs 2-Pair powering. Set to 0 if PSE always 4-Pair powers, 1 if Alt-A Pairset powered, 2 if Alt-B Pairset powered.
PRI_4pr_Pairset	Primary (PRI) Pairset where Classification occurs given Single Signature PD connection. 1= Alt-A Pairset, 2= Alt-B Pairset, 12= Either Pairset.

class_err — PSE Processing of Deviant Class Signatures

Evaluates PSE current limiting to very high class and mark loads and PSE powering response to current limited signatures and to invalid class signature sequences.

Class_Ilim_A	Classification Event current limit on the Alt-A Pairset.
Class_Ilim_B	Classification Event current limit on the Alt-B Pairset.
Pwr_Cl_52_SS	Flag indicating if PSE powers a 52mA Class signature given a Single Signature PD. 0= No Power. 1= Power Applied.
Pwr_Cl_52_DSA	Flag indicating if PSE powers the Alt-A Pairset a 52mA Class signature given a Dual Signature PD. 0= No Power. 1= Power Applied.
Pwr_Cl_52_DSB	Flag indicating if PSE powers the Alt-B Pairset a 52mA Class signature given a Dual Signature PD. 0= No Power. 1= Power Applied.
Class_Reset_SS	Flag indicating if PSE produces at least 15msec of IDLE time and voltage on both pairsets following and aborted classification sequence with a single signature PD.
Class_Reset_DS	Flag indicating if PSE produces at least 15msec of IDLE time and voltage on each pairset following aborted classification sequences with a dual signature PD.
Mark_Ilim_A	Mark Event current limit on the Alt-A Pairset.
Mark_Ilim_B	Mark Event current limit on the Alt-B Pairset.

Classification Probing and Functional Tests

Inval_Sig_EV2_SS	Flag indicating if the PSE powers an uneven 2-Event classification given a Single Signature PD where Event 1 is 40mA, Event 2 is 18 mA. 0 = No Power, 1= Power Applied. =0 for 1-Event PSE.
Inval_Sig_EV4_SS	Flag indicating if the PSE powers an uneven 4-Event classification given a Single Signature PD where Event #4 differs from Event #3. 0 = No Power, 1= Power Applied. =0 for < 4-Event PSE.
Inval_Sig_EV5_SS	Flag indicating if the PSE powers an uneven 5-Event classification given a Single Signature PD where Event #5 differs from Event #4. 0 = No Power, 1= Power Applied. =0 for < 5-Event PSE.
Inval_Sig_EV2_DSA	Flag indicating if the PSE powers the Alt-A Pairset following an uneven 2-Event classification given a Dual Signature PD. 0 = No Power, 1= Power Applied.
Inval_Sig_EV2_DSB	Flag indicating if the PSE powers the Alt-B Pairset following an uneven 2-Event classification given a Dual Signature PD. 0 = No Power, 1= Power Applied. =0 for 1-Event PSE.
Inval_Sig_EV4_DSA	Flag indicating if the PSE powers the Alt-A Pairset following an uneven 4-Event classification where Event #4 differs from Event #3 given a Dual Signature PD. 0 = No Power, 1= Power Applied.
Inval_Sig_EV4_DSB	Flag indicating if the PSE powers the Alt-B Pairset following an uneven 4-Event classification where Event #4 differs from Event #3 given a Dual Signature PD. 0 = No Power, 1= Power Applied.

class_lldp — LLDP Protocol & Power Grant Testing Emulating Single Signature PD's

Assesses 802.3bt PSE LLDP (29 octet) basic protocol fields, protocol timing, and power request processing for 802.3bt single signature PD's. (*Requires LLDP Emulation & Analysis feature license*.)

PSE_LLDP_Time_SS	Time from Power On to 1st LLDP Frame. -1 = No Frame Received < 45 seconds
LLDP_Length	TLV Length Field. 29 for 802.3bt
PSE_Pwr_Pair	MDI Legacy Powered Pair. Confirm the value of either 1 or 2. All other values fail. Value = 1 means the Signal Pairs are in use. Value = 2 means the Spare Pairs are in use.
PSE_MDI_Pwr_Sup	MDI Power Support Field. 4 bit value where bits 0-2 are set and bit 3 is don't care.
PSE_Pwr_Class	MDI 802.3at PSE Class Support. Class 4 and above will specify 4
PSE_Source_Priority	MDI 802.3at Type-Source-Priority field. If PSE is Type-3 and Type-4 it will specify Type-2
PSE_Ext_Type	Extended PSE Type. Either Type-3 or Type-4
PSE_Ext_Status_SS	Powering Status of PSE. =41 if set to Both_Alts and 4pr_Pwr_Single =21 if et to Alt_A or Alt_B and 2pr_Pwr. Otherwise set to 0.
PSE_Ext_Class_SS	Assigned Class available from the PSE. =41 if Class between 1 and 8 and 4pr_Pwr_Single. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0
PSE_Max_Pwr_SS	Reported PSE maximum available port power. There are no restrictions on this value.
PSE_Class_6_Ext_Pwr	Flag indicating that PSE allows extended power allocations to a Class 6 PD. If PSE_Max_Pwr_SS reports > 51.0 watts, a class 6 LLDP power request exceeding 51.0 watts is performed. 0 = Power Allocation limited to 51.0 watts and 1= Power Allocation exceeded 51.0 watts.
PSE_Pwr_Class_DS	Value of the Dual-sig Extended Class for Alt-A and Alt-B. Set to 1 if both TLVs are set to Single Signature otherwise set to 0.
PSE_Echo_Time_1SS	Time from a PD request for an initial power until the frame containing the Echo of that request is received
PSE_Alloc_Time_1SS	Time from a PD request for an initial power until the frame containing the Allocation of that request is received
PSE_Alloc_LowPwr_1SS	Power Allocated by the PSE when requesting an initial power
PSE_Echo_Time_2SS	Time from a PD request for a change to the max power available until the frame containing the Echo of that request is received
PSE_Alloc_Time_2SS	Time from a PD request for a change to the max power available until the frame containing the Allocation of that request is received
PSE_Alloc_MaxPwr_2SS	Indicates Power was Allocated by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated
PSE_AT_Pwr_Neg	Flag indicating that PSE supports 802.3at PoE TLV's (12-octet) protocol.
PSE_Post_AT_Pwr_Neg	Flag indicating that PSE will return to 802.3bt PoE TLV's following a prior PD connection that negotiated using 802.3at PoE TLV's.
Link_Down_Shutdown	Disconnect the LAN. Set to 1 if Power NOT removed. 0 if Power removed

Classification Probing and Functional Tests

class_lldp2 — LLDP Protocol & Power Grant Testing Emulating Dual Signature PD's

Assesses 802.3bt PSE LLDP (29 octet) basic protocol fields, protocol timing, and power request processing for 802.3bt dual signature PD's. (*Requires LLDP Emulation & Analysis feature license*.)

PSE_LLDP_Time_DS	Time from Power On to 1st LLDP Frame. -1 = None Received < 45 sec.
PSE_Ext_Status_DS	Powering Status of PSE. =42 if set to Both_Alts and 4pr_Pwr_Dual =21 if et to Alt_A or Alt_B and 2pr_Pwr. Otherwise set to 0.
PSE_Ext_Class_DSA	Assigned Class available from the PSE on Alt-A. =42 if Class between 1 and 5 and 4pr_Pwr_Dual. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0
PSE_Ext_Class_DSB	Assigned Class available from the PSE on Alt-B. =42 if Class between 1 and 5 and 4pr_Pwr_Dual. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0
PSE_Max_Pwr_DS	Reported PSE maximum available port power. There are no restrictions on this value. Value is the sum of both pairsets.
PSE_Pwr_Class_SS	Value of the Single-sig Extended Class for Alt-A and Alt-B. Set to 1 if TLV is set to Single Signature otherwise set to 0.
PSE_Echo_Time_1DS	Time from a PD request for a change to a low power until the frame containing the Echo of that request is received
PSE_Alloc_Time_1DS	Time from a PD request for a change to a low power until the frame containing the Allocation of that request is received
PSE_Alloc_LowPwr_1DSA	Power Allocated on Alt-A by the PSE when requesting a change to a low power
PSE_Alloc_LowPwr_1DSB	Power Allocated on Alt-B by the PSE when requesting a change to a low power
PSE_Echo_Time_2DS	Time from a PD request for a change to the max power available until the frame containing the Echo of that request is received
PSE_Alloc_Time_2DS	Time from a PD request for a change to the max power available until the frame containing the Allocation of that request is received
PSE_Alloc_MaxPwr_2DSA	Indicates Power was Allocated on Alt-A by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated
PSE_Alloc_MaxPwr_2DSB	Indicates Power was Allocated on Alt-B by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated
PSE_Alloc_Limit_DS	Flag indicating if PSE will over-allocate to a Class 3 D power-up. 1 = max allocation consistent with assigned pairset classe. 0= allocation exceeded pairset assigned classes.

Power-Up Processes

pwrup_time — Power-Up Timing Parameters

Measures power-up rise time and time delay from completion of detection until POWER_ON state.

Pwr_On_Time_Tpon_SS	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state given a Single Signature PD.
Pwr_On_Time_Tpon_DSA	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state on the Alt-A Pairset given a Dual Signature PD.
Pwr_On_Time_Tpon_DSB	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state on the Alt-B Pairset given a Dual Signature PD.
Pwrup_Rise_Time_A	Estimated time (µsec) for the Alt-A Pairset to transit from 10% of Vpse to 90% of Vpse while applying power.
Pwrup_Rise_Time_B	Estimated time (µsec) for the Alt-B Pairset to transit from 10% of Vpse to 90% of Vpse while applying power.
Pwr_Stagger_Time_SS4	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up given Single Signature Class 4. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.
Pwr_Stagger_Time_SS5	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up given Single Signature Class 5. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.
Pwr_Stagger_Time_DS	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up

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given Dual Signature PD. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.

pwrup_inrush — PSE Current Limiting Behaviors During Power-Up

Evaluates PSE current limiting and inrush overload tolerance parameters. Assures compliance to 802.3bt figure 145-22, IInrush current and timing limits in the POWER_UP state.

Iinrush_min_Class_3	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 3 PD
Iinrush_min_Class_5	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 5 PD
Iinrush_min_Class_7	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 7 PD
Iinrush_min_Class_1D_A	Minimum Alt-A Pairset Inrush current from power-up until 50msec after power-up given Dual Signature Class PD
Iinrush_min_Class_1D_B	Minimum Alt-B Pairset Inrush current from power-up until 50msec after power-up given Dual Signature Class PD
Iinrush_4P_max_Class_3	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 3 PD
Iinrush_4P_max1_Class_5	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 5 PD and given a PSE that grants a maximum of Class 4 power.
Iinrush_4P_max2_Class_5	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 5 PD and given a PSE that grants greater than Class 4 power.
Iinrush_4P_max1_Class_7	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants a maximum of Class 4 power.
Iinrush_4P_max2_Class_7	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants greater than Class 4 power.
Iinrush_2P_max_Class_3	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 3 PD.
Iinrush_2P_max1_Class_7	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants a maximum of Class 4 power.
Iinrush_2P_max2_Class_7	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants greater than Class 4 power.
Iinrush_2p_max_Cl_1D_A	Maximum 2-Pair Inrush current on the Alt-A Pairset from 1msec after power-up until shutdown given a Dual Signature Class 1 PD.
Iinrush_2p_max_Cl_1D_B	Maximum 2-Pair Inrush current on the Alt-B Pairset from 1msec after power-up until shutdown given a Dual Signature Class 1 PD.
Tinrush_minPr_Class_3	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 3 PD - minimum of the Alt-A and Alt-B Pairsets
Tinrush_maxPr_Class_3	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 3 PD - maximum of the Alt-A and Alt-B Pairsets
Tinrush_minPr_Class_7	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 7 PD - minimum of the Alt-A and Alt-B Pairsets
Tinrush_maxPr_Class_7	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 7 PD - maximum of the Alt-A and Alt-B Pairsets
Tinrush_Class_1D_A	Inrush Shutdown Time measured from power-up until power removal on the Alt-A Pairset given Dual Signature Class 1 PD
Tinrush_Class_1D_B	Inrush Shutdown Time measured from power-up until power removal on the Alt-B Pairset given Dual Signature Class 1 PD
Delay_Inrush_Class_7	Inrush Shutdown Time measured from power-up until power removal on both Pairsets given a Single Signture Class 7 PD and an inrush overload that is delayed by 25msec from power-up
Delay_Inrush_Class_2D_A	Inrush Shutdown Time measured on the Alt-A Pairset from power-up until power removal given a Dual Signture Class 1 PD and an inrush overload that is delayed by 25msec from power-up of the Alt-A Pairset
Delay_Inrush_Class_2D_B	Inrush Shutdown Time measured on the Alt-B Pairset from power-up until power removal given a Dual Signture Class 1 PD and an inrush overload that is delayed by 25msec from power-up of the Alt-B Pairset
45ms_Pwr_Stat_Class_7	Flag indicating if PSE maintained power when a 45msec Inrush current overload is applied given a Single Signature Class 7 PD. 1= Power Maintained, 0= Power Removed.
45ms_Pwr_Stat_Class_2D_A	Flag indicating if PSE maintained power on the Alt-A Pairset when a 45msec Inrush current overload is applied given a Dual Signature Class 2 PD. 1= Power Maintained, 0= Power Removed.

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45ms_Pwr_Stat_Class_2D_B	Flag indicating if PSE maintained power on the Alt-B Pairset when a 45msec Inrush current overload is applied given a Dual Signature Class 2 PD. 1= Power Maintained, 0= Power Removed.
Vinrush_Class_2D_A	Inrush voltage on the Alt-A Pairset while the PSE is in current limit.
Vinrush_Class_2D_B	Inrush voltage on the Alt-B Pairset while the PSE is in current limit.
Inrush_16V_DS3A	Inrush current supplied when inrush voltage drops to 16V (i.e. <<30V) on the Alt-A pairset.
Inrush_16V_DS3B	Inrush current supplied when inrush voltage drops to 16V (i.e. <<30V) on the Alt-B pairset.

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pwron_v — Powered Port Voltages, Ripple, and Noise

Measures PSE port DC and AC voltages in response to minimum and maximum power loads.

Vpse_Max_Alt_A	PSE output voltage on the Alt-A Pairset when PSE is powered and lightly loaded (~1W).
Vpse_Max_Alt_B	PSE output voltage on the Alt-B Pairset when PSE is powered and lightly loaded (~1W).
Vpse_Min_Alt_A	PSE output voltage on the Alt-A Pairset when PSE is powered and heavily loaded (~95% of Pclass).
Vpse_Min_Alt_B	PSE output voltage on the Alt-B Pairset when PSE is powered and heavily loaded (~95% of Pclass).
Vport_PSE_diff=	Difference between Alt-A and Alt-B output voltages when PSE is 4-pair powered and has zero mA load.
V_ripple_A	Low frequency (20Hz-150Hz) ripple measured on the Alt-A Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.
V_ripple_B	Low frequency (20Hz-150Hz) ripple measured on the Alt-B Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.
V_noise_A	High frequency (50KHz-300KHz) noise measured on the Alt-A Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.
V_noise_B	High frequency (50KHz-300KHz) noise measured on the Alt-B Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.
V_trans_A	Minimum voltage measured on the Alt-A Pairset during a load transition from ~0.5W to ~Pclass and back over a short (< 5msec) duration.
V_trans_B	Minimum voltage measured on the Alt-B Pairset during a load transition from ~0.5W to ~Pclass and back over a short (< 5msec) duration.

pwron_pwrcap — PSE Port Static Power Capacity

Measures the maximum power delivery capability of a PSE port given various PD Classifications and LLDP power allocations.

Max_Asgn_Class_SS	The maximum classification a PSE will assign to a Single Signature PD through either event counts or LLDP. (*LLDP emulations require the PSA-LLDP feature license*.)
Pcon_c1	Maximum sustained power (in watts) to a Class 1 PD
Icon_%_c1	Maximum sustained load current as a % of **Icon** for a Class 1 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c2	Maximum sustained power (in watts) to a Class 2 PD
Icon_%_c2	Maximum sustained load current as a % of **Icon** for a Class 2 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c3	Maximum sustained power (in watts) to a Class 3 PD
Icon_%_c3	Maximum sustained load current as a % of **Icon** for a Class 3 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c4	Maximum sustained power (in watts) to a Class 4 PD
Icon_%_c4	Maximum sustained load current as a % of **Icon** for a Class 4 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c5	Maximum sustained power (in watts) to a Class 5 PD
Icon_%_c5	Maximum sustained load current as a % of **Icon** for a Class 5 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c6	Maximum sustained power (in watts) to a Class 6 PD
Icon_%_c6	Maximum sustained load current as a % of **Icon** for a Class 6 PD, the minimum required load

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	current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c7	Maximum sustained power (in watts) to a Class 7 PD
Icon_%_c7	Maximum sustained load current as a % of **Icon** for a Class 7 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Pcon_c8	Maximum sustained power (in watts) to a Class 8 PD
Icon_%_c8	Maximum sustained load current as a % of **Icon** for a Class 8 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.
Type_N_Enable	Powering status when a load of ~ 90% **Pclass** (Icon) is applied at 80 msec following power-up.
Pclass_LLDP_95%	LLDP Granting PSE's Only: Power status when a negotiation for 95% of the maximum available PSE port power is negotiated, then the corresponding PD load with maximum cable loss is applied.
Pclass_LLDP_75%	LLDP Granting PSE's Only: Power status when a negotiation for 75% of the maximum available PSE port power is negotiated, then the corresponding PD load with maximum cable loss is applied.
Max_Asgn_Class_DS	The maximum classifications a PSE will assign to a Dual Signature PD (on both pairsets) through either event counts or LLDP.
Pcon_c1DA	Maximum sustained power on the Alt-A pairset (in watts) to a Dual Class 1 PD
Icon_%_c1DA	Given a Dual Class 1 PD, the maximum sustained Alt-A load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.
Pcon_c2DB	Maximum sustained power on the Alt-B pairset (in watts) to a Dual Class 2 PD
Icon_%_c2DB	Given a Dual Class 2 PD, the maximum sustained Alt-B load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.
Pcon_c3DA	Maximum sustained power on the Alt-A pairset (in watts) to a Dual Class 3 PD
Icon_%_c3DA	Given a Dual Class 3 PD, the maximum sustained Alt-A load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.
Pcon_c4DB	Maximum sustained power on the Alt-B pairset (in watts) to a Dual Class 4 PD
Icon_%_c4DB	Given a Dual Class 4 PD, the maximum sustained Alt-B load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.
Pcon_c5DA	Maximum sustained power on the Alt-A pairset (in watts) to a Dual Class 4 PD
Icon_%_c5DA	Given a Dual Class 4 PD, the maximum sustained Alt-A load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.

pwron_unbal — PSE Port Pair-to-Pair Unbalance Tolerance

Assesses PSE ability to support worst case pairset-to-pairset unbalanced loading given single signature PD emulations.

pseP2pUnbal_c4A	If a PSE powers Class 4 with 4-Pairs: The powering status when a total load of ~90% Icon is shifted onto the Alt-A pairset and the load current on the Alt-B pairset is zero mA. 0= Unpowered, 1= Powered.
pseP2pUnbal_c4B	If a PSE powers Class 4 with 4-Pairs: The powering status when a total load of ~90% Icon is shifted onto the Alt-B pairset and the load current on the Alt-A pairset is zero mA. 0= Unpowered, 1= Powered.
pseP2pUnbal_c5A **pseP2pUnbal_c6A** **pseP2pUnbal_c7A** **pseP2pUnbal_c8A**	The powering status when a total load of ~90% **Icon** is split such that the Alt-A pairset gets **Icon_2p_unb** and the Alt-B pairset gets the remaining load current (90% * **Icon** - **Icon_2p_unb**). **Icon_2p_unb** = 560mA for assigned class 5, 692mA for assigned class 6, 794mA for assigned class 7, and 948mA for assigned class 8. 0= Unpowered, 1= Powered.
pseP2pUnbal_c5B **pseP2pUnbal_c6B** **pseP2pUnbal_c7B** **pseP2pUnbal_c8B**	The powering status when a total load of ~90% **Icon** is split such that the Alt-B pairset gets **Icon_2p_unb** and the Alt-A pairset gets the remaining load current (90% * **Icon** - **Icon_2p_unb**). **Icon_2p_unb** = 560mA for assigned class 5, 692mA for assigned class 6, 794mA for assigned class 7, and 948mA for assigned class 8. 0= Unpowered, 1= Powered.
pseP2pPkUnbal_A **pseP2pPkUnbal_B**	The powering status following an **Ipeak_2p_unb** (= **Ilim_2p** - 2mA) transient load of duration **Tcut_min** (50msec) applied to the pairset (Alt-A or Alt-B) that is carrying the higher unbalanced load at PSE maximum supported class.

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pwron_maxi — PSE Response to Maximum Overloads

Evaluates PSE characteristics with respect to the POWER_ON state PI operating current templates in Figures 145-23 and 145-24 of the 802.3bt specification.

Ilim_2p_max_SSA	Maximum pairset current measured during “short circuit” overload from the maximum single signature class PD that the PSE will grant full power to. Assessed on both the Alt-A and Alt-B pairsets.
Ilim_2p_max_SSB	
Tlim_SS	Time from short circuit overload assertion until first pairset shutdown. The low side of this parameter is not enforceable because the standard allows that when PSE output voltage drops below **Vport_pse_2p**(Min), the PSE may remove power without regard to Tlim. A PSE that is limiting output current would almost certainly drop output voltage below **Vport_pse_2p**(min).
Ilim_2p_max_DSA	Maximum pairset current measured during “short circuit” overload from the maximum dual signature class PD that the PSE will grant full power to. Assessed on both the Alt-A and Alt-B pairsets.
Ilim_2p_max_DSB	
Tlim_DSA	Time from short circuit overload assertion until Alt-A pairset shutdown. See Tlim_SS above.
Tlim_DSB	Time from short circuit overload assertion until Alt-B pairset shutdown. See Tlim_SS above.
Ilim_min_cAB3	Minimum current sustained with **Ilim_min_2p** (400mA) applied to Alt-A, then to Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c3	PSE Powering status 100msec after class 3 **Ilim_min_2p** transient was applied for **Tlim_min** on each pairset. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB4	Minimum current sustained with **Ilim_min_2p** (684mA) applied to Alt-A, then to Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c4	PSE Powering status 100msec after class 4 **Ilim_min_2p** transient was applied for **Tlim_min** on each pairset. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB5	Minimum current sustained with **Ilim_min_2p** (580mA) applied simultaneously to Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c5	PSE Powering status 100msec after class 5 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB6	Minimum current sustained with **Ilim_min_2p** (720mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c6	PSE Powering status 100msec after class 6 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB7	Minimum current sustained with **Ilim_min_2p** (850mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c7	PSE Powering status 100msec after class 7 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB8	Minimum current sustained with **Ilim_min_2p** (1005mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c8	PSE Powering status 100msec after class 8 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB3D	Minimum current sustained with **Ilim_min_2p** (400mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c3D	PSE Powering status 100msec after dual class 3 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB4D	Minimum current sustained with **Ilim_min_2p** (684mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c4D	PSE Powering status 100msec after dual class 4 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Ilim_min_cAB5D	Minimum current sustained with **Ilim_min_2p** (990mA) applied Alt-A and Alt-B pairsets for **Tlim_min**. Reports the minimum of both pairsets.
Max_trans_c5D	PSE Powering status 100msec after dual class 5 **Ilim_min_2p** transient was applied for **Tlim_min** on both pairsets. 1= PSE did not remove power. 0= Power was removed.
Vtrans_2p_A	Minimum Alt-A voltage in response to a maximum transient overload (Ilim_min) of 250usec duration from the maximum class PD a PSE will grant full power to.
Vtrans_2p_B	Minimum Alt-B voltage in response to a maximum transient overload (Ilim_min) of 250usec duration from the maximum class PD a PSE will grant full power to.
Iport_max_type3	Flag indicating power removed from both pairsets of Type-3 PSE with 852mA per pairset for > 75 msec. 0= Power removed, 1= Powered after 75 msec.

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Iport_max_type4	Flag indicating power removed from both pairsets of Type-4 PSE with 1302mA per pairset for > 75 msec. 0= Power removed, 1= Powered after 75 msec.
Ilps_type4	Flag indicating power removed from both pairsets of Type-4 PSE with Maximum LPS current per pairset for > 4 sec. Maximum LPS current is the current that restricts PSE to <100 Watt output. 0= Power removed, 1= Powered after 4 sec.

pwron_overld — PSE Response to Maximum PD Power Transients

Assesses powered PSE port behaviors with respect to Ipeak, the maximum power overload allowed to a PD as defined in Equation 145-11 of the 802.3bt standard.

Ipeak_c1	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 1 PD. 1= Powered, 0= Not powered.
Ipeak_c2	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 2 PD. 1= Powered, 0= Not powered.
Ipeak_c3	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 3 PD. 1= Powered, 0= Not powered.
Vport_Ipeak_c3	Minimum voltage during **Ipeak** Class 3 transient.
Ipeak_5%DC_c3	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 3 PD. 1= Powered, 0= Not powered.
Ipeak_c4	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 4 PD
Vport_Ipeak_c4	Minimum voltage during **Ipeak** Class 4 transient
Ipeak_5%DC_c4	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 4 PD. 1= Powered, 0= Not powered.
Ipeak_c5	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 4 PD. 1= Powered, 0= Not powered.
Vport_Ipeak_c5	Minimum voltage during **Ipeak** Class 5 transient
Ipeak_5%DC_c5	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 4 PD. 1= Powered, 0= Not powered.
Ipeak_c6	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 6 PD. 1= Powered, 0= Not powered.
Vport_Ipeak_c6	Minimum voltage during **Ipeak** Class 6 transient
Ipeak_5%DC_c6	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 6 PD. 1= Powered, 0= Not powered.
Ipeak_c7	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 7 PD. 1= Powered, 0= Not powered.
Vport_Ipeak_c7	Minimum voltage during **Ipeak** Class 7 transient
Ipeak_5%DC_c7	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 7 PD. 1= Powered, 0= Not powered.
Ipeak_c8	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 8 PD. 1= Powered, 0= Not powered.
Vport_Ipeak_c8	Minimum voltage during **Ipeak** Class 8 transient
Ipeak_5%DC_c8	Flag indicating if PSE maintains 13ppli following a 5% duty cylcle transient load of **Ipeak** to a Class 8 PD. 1= Powered, 0= Not powered.
Ipeak_c1D	Flag indicating if the PSE maintains power following **Ipeak_2p** current transients of duration **Tcut_min** (50msec) applied to both pairsets of a Dual Class 1 PD. 1= Powered, 0= Not powered.
Ipeak_c2D	Flag indicating if the PSE maintains power following **Ipeak_2p** current transients of duration **Tcut_min** (50msec) applied to both pairsets of a Dual Class 2 PD. 1= Powered, 0= Not powered.
Ipeak_c3D	Flag indicating if the PSE maintains power following **Ipeak_2p** current transients of duration **Tcut_min** (50msec) applied to both pairsets of a Dual Class 3 PD. 1= Powered, 0= Not powered.
Ipeak_c4D	Flag indicating if the PSE maintains power following **Ipeak_2p** current transients of duration **Tcut_min** (50msec) applied to both pairsets of a Dual Class 4 PD. 1= Powered, 0= Not powered.
Ipeak_c5D	Flag indicating if the PSE maintains power following **Ipeak_2p** current transients of duration **Tcut_min** (50msec) applied to both pairsets of a Dual Class 5 PD. 1= Powered, 0= Not powered.

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pwron_autoclass — PSE Power Capacity In Response to Autoclass Signatures

Assesses powered PSE response to various PD autoclass signatures and if the PSE is autoclass capable, determines that the PSE supports the minimum required PD load power including autoclass power margins.

Autoclass_Shutdown	PSE load is set to 95% of **Pclass** (based on assigned class) to determine if PSE removes power following an auto class signature. 0= no autoclass support, 1= apparent autoclass support.
Pac_margin_C3_low	Flag indicating that given class 3 PD autoclass load of 3W, PSE supports Pclass of 3.5W or higher (0.5W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Pac_margin_C3_high	Flag indicating that given class 3 PD autoclass load of 9W, PSE supports Pclass of 9.5W or higher (0.5W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Pac_margin_C5_low	Flag indicating that given class 5 PD autoclass load of 3W, PSE supports Pclass of 3.75W or higher (0.75W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Pac_margin_C5_high	Flag indicating that given class 5 PD autoclass load of 34W, PSE supports Pclass of 34.75W or higher (0.75W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Pac_margin_C7_low	Flag indicating that given class 7 PD autoclass load of 3W, PSE supports Pclass of 4.5W or higher (1.5W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Pac_margin_C7_high	Flag indicating that given class 7 PD autoclass load of 55W, PSE supports Pclass of 56.5W or higher (1.5W margin). Set to -1 if PSE Autoclass_Shutdown= 0.
Autoclass_4W	Flag (0, 1, or -1) indicating that an autoclass signature of less than 4W is ignored whereupon PSE furnishes assigned class from classification.

MPS Processes for Power Removal on PD Disconnect

mps_dc_valid — Valid DC MPS Load Thresholds and Tolerances

Evaluates PSE DC current thresholds for 4-pair and pairset power removal and PSE tolerance of low power MPS conditions.

Ihold_c3	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 3 PD. Report -1 if PSE only does 2-Pair power with Class 3.
Ihold_2p_c3A	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 3 PD. If PSE powers with 4-pairs, the Alt-B pairset will be drawing 1.5 mA during the scan. Set to -1 for any unpowered pairset.
Ihold_2p_c3B	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 3 PD. If PSE powers with 4-pairs, the Alt-A pairset will be drawing 1.5 mA during the scan.
Ihold_c5	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 5 PD
Ihold_2p_c5A	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 5 PD when the Alt-B pairset is drawing 1.5 mA
Ihold_2p_c5B	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 5 PD when the Alt-A pairset is drawing 1.5 mA
Ihold_c7	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 7 PD
Ihold_2p_c7A	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 7 PD when the Alt-B pairset is drawing 1.5 mA
Ihold_2p_c7B	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 7 PD when the Alt-A pairset is drawing 1.5 mA
Ihold_2p_c2DA	Minimum Alt-A load current to maintain power on the Alt-A pairset given a dual signature PD and 80mA load on the Alt-B pairset.
Ihold_2p_c2DB	Minimum Alt-B load current to maintain power on the Alt-B pairset given a dual signature PD and 80mA load on the Alt-A pairset.
LP_MPS_Tol_c3	Flag indicating if 2-Pair or 4-Pair power is applied following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 3 PD. 1= Powered, 0= Power removed.
LP_MPS_Tol_c5	Flag indicating if 4-Pair power is applied following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 5 PD. 1= Powered, 0= Power removed.
LP_MPS_Tol_c7	Flag indicating if 4-Pair power is applied following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 7 PD. 1= Powered, 0= Power removed.

MPS Processes for Power Removal on PD Disconnect

LP_MPS_Tol_c2D	Flag indicating if power is applied on both pairsets following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 2D PD. 1= Powered, 0= Power removed.

mps_dc_pwrdn — Disconnect Shutdown Timing

Evaluates disconnect shutdown timing given single and dual signature emulations and invalid MPS signatures.

Tmpdo_c3A	Time from PD disconnect until power removal on Alt-A pairset given a Class 3 PD. Tested using a load current of **Ihold_min** – 1 mA. Set to -1 if PSE only powers the Alt-B pairset.
Tmpdo_c3B	Time from PD disconnect until power removal on Alt-B pairset given a Class 3 PD. Tested using a load current of **Ihold_min** – 1 mA. Set to -1 if PSE only powers the Alt-A pairset.
Tmpdo_c5A	Time from PD disconnect until power removal on Alt-A pairset given a Class 5 PD. Tested using a load current of **Ihold_min** – 1 mA.
Tmpdo_c5B	Time from PD disconnect until power removal on Alt-B pairset given a Class 5 PD. Tested using a load current of **Ihold_min** – 1 mA.
Tmpdo_c7A	Time from PD disconnect until power removal on Alt-A pairset given a Class 7 PD. Tested using a load current of **Ihold_min** – 1 mA.
Tmpdo_c7B	Time from PD disconnect until power removal on Alt-B pairset given a Class 7 PD. Tested using a load current of **Ihold_min** – 1 mA.
Tmpdo_c2DA	Time from Alt-A pairset disconnect until power removal on the Alt-A pairset given a dual Class 2 PD. Tested using load current of **Ihold_2p_min** – 1 mA.
4pr_Stat_c2DA	Flag indicating if PSE removes power on one pairset or both pairsets when the Alt-A pairset is disconnected. 0= No power, 1= Alt-B powered, 2= Alt-A powered.
Tmpdo_c2D	Time from Alt-B pairset disconnect until power removal on the Alt-B pairset given a dual Class 2 PD. Tested using load current of **Ihold_2p_min** – 1 mA.
4pr_Stat_c2DB	Flag indicating if PSE removes power on one pairset or both pairsets when the Alt-B pairset is disconnected.

PSE Power-Down Characteristics

pwrdn_time — Discharge Time and Output Capacitance

Evaluates PSE disconnect discharge timing as well as output characteristics during power removal.

Turnoff_time_Toff_A	PSE shutdown time on the Alt-A pairset following a PD Disconnect. The measurement is performed with a hypothetical 320KΩ load 15pplied across the pairset. Measured Cout_A and Output_Rp_A values enable the decay time modeling used to produce Toff.
Turnoff_time_Toff_B	PSE shutdown time on the Alt-B pairset following a PD Disconnect. The measurement is performed with a hypothetical 320KΩ load 15pplied across the pairset. Measured Cout_B and Output_Rp_B values enable the decay time modeling used to produce Toff.
Cout_A	PSE output capacitance on the Alt-A pairset measured during disconnect shutdown.
Cout_B	PSE output capacitance on the Alt-B pairset measured during disconnect shutdown.
Output_Rp_A	PSE discharge resistance on the Alt-A pairset measured during disconnect shutdown.
Output_Rp_B	PSE discharge resistance on the Alt-B pairset measured during disconnect shutdown.
Idle_time_SS	Duration of IDLE state voltage (< 2.8V) following disconnect shutdown of a Single Signature PD

pwrdn_v — Error Delay Timing

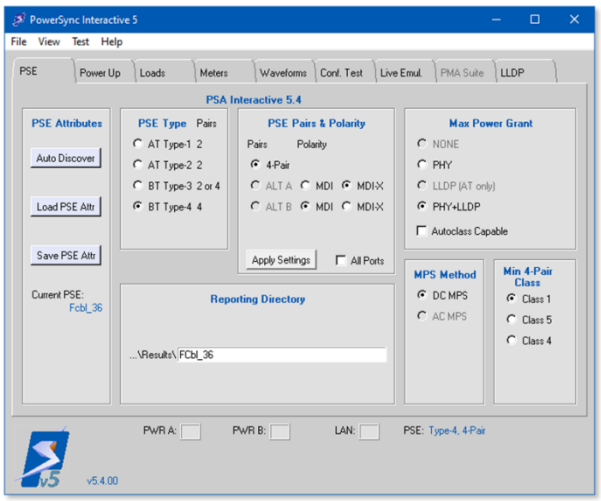
Measures PSE port time delay between an overload shutdown and restoration of PD power.

Error_Delay_SS_A	Time between overload shutdown and attempted new detection of a single signature PD on the Alt-A pairset.
Error_Delay_SS_B	Time between overload shutdown and attempted new detection of a single signature PD on the Alt-B pairset.
Error_Delay_DS_A	Time between overload shutdown and attempted new detection of a dual signature PD on the Alt-A pairset.
Error_Delay_DS_B	Time between overload shutdown and attempted new detection of a dual signature PD on the Alt-B pairset.
Idle_Voff_SS_A	Average voltage during the error delay period on the Alt-A pairset given a single signature PD
Idle_Voff_SS_B	Average voltage during the error delay period on the Alt-B pairset given a single signature PD
Idle_Voff_DS_A	Average voltage during the error delay period on the Alt-A pairset given a dual signature PD
Idle_Voff_DS_B	Average voltage during the error delay period on the Alt-B pairset given a dual signature PD

Configuring and Running the 4-Pair PSE Conformance Test Suite

The 4-Pair PSE Conformance Test Suite is accessed from both PSA Interactive Software (GUI) and PowerShell PSA, an extended Tcl/Tk command line shell.

Within **PSA Interactive**, two menus are relevant to the PSE Conformance Test Suite. First, the **PSE** tab menu allows users to describe, discover, or load previously stored PSE Attributes. These parameters are critical to the behavior of the PSE 4-Pair Conformance Test Suite and must be properly established for any PSE to be tested.



PSA Interactive PSE Tab Menu

PSE attributes include **PSE Type** (e.g. Type-3 or Type-4), **PSE Pairs** (4-Pair), **PSE Polarity** (MDI or MDI-X on each pairset), **Max Power Grant** method (PHY or PHY+LLDP), **Autoclass Capability**, **MPS Method** (DC), and **Min. 4-Pair Class** (1, 4, or 5). If these attributes are not properly declared and applied, then PSE conformance test sequencing may produce inappropriate or missing parameters and incorrect limit checking. PSE attributes (excluding **Autoclass Capability**) can be automatically discovered from a connected PSE port using the **Auto Discover** menu. They can be saved for future recall using the **Save PSE Attr** control and they can be recalled and applied to the PSA instrument by using the **Load PSE Attr** control.

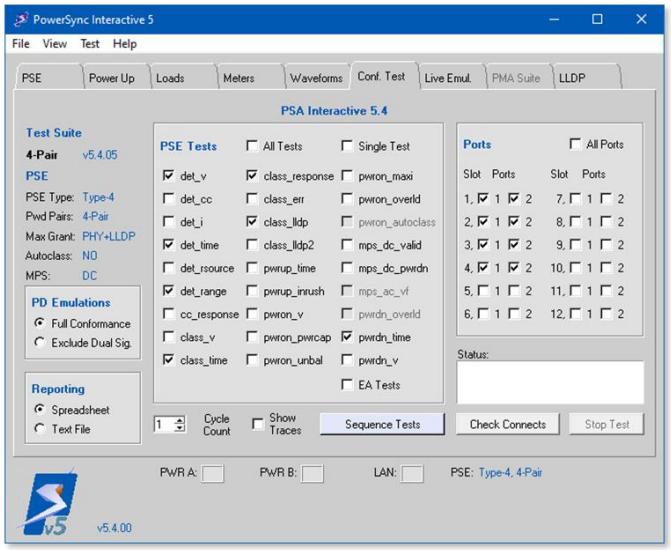
The presently described **PSE Type** and **Powered Pairs** is always displayed in blue in the lower right. The 4-Pair PSE Conformance Test Suite will only be activated when this indicator displays Type-3, 4-Pair or Type-4, 4-Pair.

The **Conf. Test** tab menu is then accessed to configure fully automated test sequences. This menu will automatically configure itself for **4-Pair** PSE testing when the most recently described PSE is Type-3, 4-Pair or Type-4, 4-Pair. Using this menu, automated sequences of selected tests across selected test ports are readily configured and initiated. Alternatively, the menu supports running just a **Single Test** on a single port.

With the **4-Pair** PSE test suite, users have the option to run **Full Conformance** testing or to run excluding Dual Signature test cases in order to speed up some of the longer tests such as **pwron_pwrcap** and **pwron_maxi**. A complete PSE conformance test would require that **All Tests** be run with the **Full Conformance** setting.

Other PSE attributes including maximum power granting method (**Max Grant**) and **Autoclass** capability correspond to settings established in the **PSE** tab menu. These attributes affect which tests are available and selectable in the menu.

User's may also select one of two reporting options when sequencing tests including the default option to produce a pop-up (Microsoft Excel) spreadsheet report for test parameter limit checking and analysis.



PSA Interactive Conformance Test Menu

Multi-Port PSE connections can rapidly be verified prior to testing from this menu using the **Check Connects** control after selecting the desired **Ports**. Additionally, users may opt to have waveform traces produced by each test appear on screen as each test runs. Test sequences may be re-cycled up to 16 times using a **Cycle Count** control for those who need to perform exhaustive QA while getting insights into intermittent PSE behaviors.

In PowerShell PSA, PSE attributes are auto-discovered using the **psa_auto_port** command and can be recalled with the **psa_pse** command. Test sequencing from PowerShell PSA is performed using the **sequence** command.

The 4-Pair PSE Conformance Test Suite Standard Report

The standard spreadsheet test report for the 4-Pair SE Conformance Test Suite provides efficient feedback by clearly notating any specification compliance violations both by test parameter and by test (PSE) port. The report also accumulates minimum, maximum, and average parameter values across PSE ports so that users can spot individual port deviations and assess performance to design goals. Multiple cycles of testing can be specified to produce one report page per sequence cycle.

All test limit processing automatically adapts the type of PSE (Type-3 or Type-4), the High Power Grant Method, and to other factors that are specified before the sequence begins. Test limit tables are found on the **Limits** page of the report.

The standard report includes a **Notes** page with detailed explanations of each parameter in each test including references to 802.3bt PICS and associated 802.3bt clauses.

The standard report also includes Sifos proprietary indexes summarizing PSE **Safety** and PSE **Interop**. These scores are derived from weighted appraisals of each test parameter in each test. Separate report tabs for Safety and Interop display the scoring performed for each index.

The report will automatically scale to the number of tested PSE ports and will produce multiple pages for multiple test cycles.

PSE Conformance Test Suite — May 15 2020 3:28 AM
Port Count: 4
Loop Count: 1
PSE Tested: Sample Type-4 4-Port PSE

Sifos Technologies — 802.3bt 4Pr Conformance Report (version 5.2.12)
PSE Type: 4 MDI-X+MDI (report version 5.2.00)
Safety Index*: 97% Interop Index*: 99%
Error Log: None

Chassis ID: 192.168.221.88
TestLoop: 1

	PSA-3000 Ports											
	1-1	1-2	2-1	2-2	UNITS	Min	Max	Average	Low Limit	P/F	High Limit	P/F
Test: det_v												
Open_Circuit_Voc_A=	15.4	14.8	15	15.4	volts	14.8	15.4	15.2	0	Pass	30	Pass
Open_Circuit_Voc_B=	15.3	15.2	15	15.1	volts	15	15.3	15.2	0	Pass	30	Pass
Backoff_Voltage_A=	1.1	1.1	1.1	1.1	volts	1.1	1.1	1.1	0	Pass	2.8	Pass
Backoff_Voltage_B=	1.3	1.3	1.2	1.2	volts	1.2	1.3	1.3	0	Pass	2.8	Pass
Backoff_Voltage_Ss=	1.4	1.4	1.5	1.5	volts	1.4	1.5	1.5	0	Pass	2.8	Pass
Max_Det_Step_V_A=	8.02	8.04	8.22	8.23	volts	8.02	8.23	8.13	3.8	Pass	10	Pass
Max_Det_Step_V_B=	8.02	8.04	8.28	8.29	volts	8.02	8.29	8.16	3.8	Pass	10	Pass
Min_Det_Step_V_A=	4.44	4.48	4.9	4.91	volts	4.44	4.91	4.68	2.8	Pass	9	Pass
Min_Det_Step_V_B=	4.48	4.48	4.95	4.96	volts	4.48	4.96	4.72	2.8	Pass	9	Pass
Det_Step_Changes_A=	3	3	3	3	---	3	3	3	1	Pass	9	Pass
Det_Step_Changes_B=	3	3	3	3	---	3	3	3	1	Pass	9	Pass
Min_Step_DV_A=	1.73	1.73	1.76	1.76	volts	1.73	1.76	1.75	1	Pass	7.2	Pass
Min_Step_DV_B=	1.71	1.72	1.77	1.76	volts	1.71	1.77	1.74	1	Pass	7.2	Pass
Pre-Det_CC_Step_V_A=	5.31	5.33	5.6	5.6	volts	5.31	5.6	5.46	0	Pass	10	Pass
Pre-Det_CC_Step_V_B=	1.86	1.87	1.82	1.82	volts	1.82	1.87	1.84	0	Pass	10	Pass
Test: det_cc												
Presumed_CC_DET_SEQ=	1	1	1	1	---	1	1	1	0	Pass	3	Pass
Conn_Chk_SS_V_A=	8.05	8.1	8.26	8.27	volts	8.05	8.27	8.17	2.8	Pass	10	Pass
Conn_Chk_SS_V_B=	8.05	8.06	8.3	8.32	volts	8.05	8.32	8.18	2.8	Pass	10	Pass
Conn_Chk_DS_V_A=	5.28	5.28	5.22	5.22	volts	5.22	5.28	5.25	2.8	Pass	10	Pass
Conn_Chk_DS_V_B=	5.31	5.31	5.26	5.26	volts	5.26	5.31	5.29	2.8	Pass	10	Pass
High_Signature_CC_A=	1	1	1	1	---	1	1	1	1	Pass	1	Pass
High_Signature_CC_B=	1	1	1	1	---	1	1	1	1	Pass	1	Pass
4Pair_Start_Fail=	0	0	0	0	---	0	0	0	0	Pass	0	Pass
Test: det_i												
Isc_Init_A=	0.34	0.36	0.29	0.34	mA	0.29	0.36	0.33	0	Pass	5	Pass
Isc_Init_B=	0.28	0.29	0.29	0.3	mA	0.28	0.3	0.29	0	Pass	5	Pass
Isc_Det_A=	0.34	0.36	0.28	0.3	mA	0.28	0.36	0.32	0	Pass	5	Pass
Isc_Det_B=	0.26	0.26	0.26	0.3	mA	0.26	0.3	0.27	0	Pass	5	Pass
Det_Slew_A=	0.0068	0.0072	0.0056	0.008	V/usec	0.0056	0.0072	0.0064	0	Pass	0.1	Pass
Det_Slew_B=	0.0052	0.0052	0.0052	0.006	V/usec	0.0052	0.006	0.0054	0	Pass	0.1	Pass
Test: det_range												
Rgood_Max_Single=	26	27	26	28	Kohm	26	28	26.8	27	Fail	32	Pass
Rgood_Min_Single=	16	16	16	16	Kohm	16	16	16	16	Pass	19	Pass
Cgood_Max_Single=	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Rgood_Max_Dual_A=	26	28	27	28	Kohm	26	28	27.3	27	Fail	32	Pass
Rgood_Max_Dual_B=	27	27	28	27	Kohm	27	28	27.3	27	Pass	32	Pass
Rgood_Min_Dual_A=	16	16	16	16	Kohm	16	16	16	16	Pass	19	Pass
Rgood_Min_Dual_B=	16	16	16	16	Kohm	16	16	16	16	Pass	19	Pass
Cgood_Max_Dual_A=	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Cgood_Max_Dual_B=	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Test: det_time												
Detect_Time_Tdet_A=	267.6	265.6	267.6	265.6	msec	265.6	267.6	266.6	0	Pass	500	Pass
Detect_Time_Tdet_B=	267.6	265.6	267.6	265.6	msec	265.6	267.6	266.6	0	Pass	500	Pass
Backoff_Time_SS=	601.6	597.7	601.6	597.7	msec	597.7	601.6	599.7	0	Pass	9999	Pass
Det2Det_Time=	382.8	378.9	382.8	380.9	msec	378.9	382.8	381.4	0	Pass	400	Pass
Test: det_rsource												
PSE_Detect_Source=	1	1	1	1	---	1	1	1	0	Pass	1	Pass
PSE_Source_Zout_A=	300	300	300	300	Kohm	300	300	300	45	Pass	300	Pass
PSE_Source_Zout_B=	300	300	300	300	Kohm	300	300	300	45	Pass	300	Pass
Test: cc_response												
Single_Sig_Response=	1	1	1	1	---	1	1	1	1	Pass	1	Pass
Dual_Sig_Response=	1	1	1	1	---	1	1	1	1	Pass	1	Pass
2Pair_PD_A=	1	1	1	1	---	1	1	1	0	Pass	2	Pass
2Pair_PD_B=	1	1	1	1	---	1	1	1	0	Pass	2	Pass
Test: class_v												
Vclass_max_SS=	18	17.8	17.8	18.1	volts	17.8	18.1	17.9	15.5	Pass	20.5	Pass
Vclass_min_SS=	17.6	17.4	17.4	17.7	volts	17.4	17.7	17.5	15.5	Pass	20.5	Pass
Vmark_SS=	8.4	8.2	8.1	8.5	volts	8.1	8.5	8.3	7	Pass	10	Pass
Vreset_SS=	-1	-1	-1	-1	---	-1	-1	-1	0	Pass	2.8	Pass
Vclass_max_DSA=	18	17.9	17.8	18.2	volts	17.8	18.2	18	15.5	Pass	20.5	Pass
Vclass_max_DSB=	18	18	17.9	18	volts	17.9	18	18	15.5	Pass	20.5	Pass
Vclass_min_DSA=	17.6	17.4	17.4	17.7	volts	17.4	17.7	17.5	15.5	Pass	20.5	Pass
Vclass_min_DSB=	17.5	17.6	17.4	17.5	volts	17.4	17.6	17.5	15.5	Pass	20.5	Pass
Vmark_DSA=	8.4	8.2	8.2	8.5	volts	8.2	8.5	8.3	7	Pass	10	Pass
Vmark_DSB=	8.3	8.3	8.3	8.3	volts	8.3	8.3	8.3	7	Pass	10	Pass
Vreset_DSA=	-1	-1	-1	-1	---	-1	-1	-1	-1	Pass	2.8	Pass
Vreset_DSB=	-1	-1	-1	-1	---	-1	-1	-1	-1	Pass	2.8	Pass
Test: class_time												
Class_Probe_SS=	0	0	0	0	---	0	0	0	0	Pass	1	Pass
EV_Count_7_SS=	5	5	5	5	Events	5	5	5	1	Pass	5	Pass
Long_EV1_Time_SS=	93.7	93.8	95.7	93.8	msec	93.7	95.7	94.3	88	Pass	105	Pass
Min_Class_EV_Time_SS=	9.7	7.8	7.8	7.8	msec	7.8	9.7	8.3	6	Pass	20	Pass
Max_Class_EV_Time_SS=	15.7	13.7	13.7	13.7	msec	13.7	15.7	14.2	6	Pass	20	Pass
Min_Mark_EV_Time_SS=	7.8	9.7	9.7	9.7	msec	7.8	9.7	9.2	6	Pass	12	Pass

PSE 4-Pair Conformance Test Suite Standard Report (excerpt)

EA Mode Testing

EA Certified 2.0™

When **EA Tests** are selected in the **Conf. Test** menu, the required PSE EA tests are automatically selected and then sequenced to a specialized EA Gen2 test report. This test report is fully secured against user edits and modifications. Manufacturers performing Gen2 EA certification testing may then submit these reports to the Ethernet Alliance's certified auditor when seeking Gen2 PoE Logo Certification for PSE's.

Ordering Information

PSA-CT4P*, 4-Pair PSE Conformance Test Suite for One PSA Address (Up to 24 Test Ports)

PSA-CT-TS1, Tracking Service, 4-Pair and 2-Pair PSE Conformance Suites for One Year for One PSA Address

PSA-CT-TS2, Tracking Service, 4-Pair and 2-Pair PSE Conformance Suites for Two Years for One PSA Address

PSA-CT-STS1, Tracking Service, 4-Pair and 2-Pair PSE Conformance Suites for One Year for Two or More PSA Addresses Operating at a Single Site

PSA-CT-STS2, Tracking Service, 4-Pair and 2-Pair PSE Conformance Suites for Two Years for Two or More PSA Addresses Operating at a Single Site

* **NOTE**: *PSA-CT4P requires one or more **PSA-3202** test blades or **PSA-3402** Compact PSA and is also supported on the **PSA-3248** RackPack PSA. Any emulation and testing of PSE LLDP behaviors further requires the **LLDP Emulation & Analysis** feature license for the PSA-3000.*

Standard spreadsheet reporting requires Microsoft Excel version 2007 or later installed on a host PC.

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Verification, Simplified.

