CORELIS

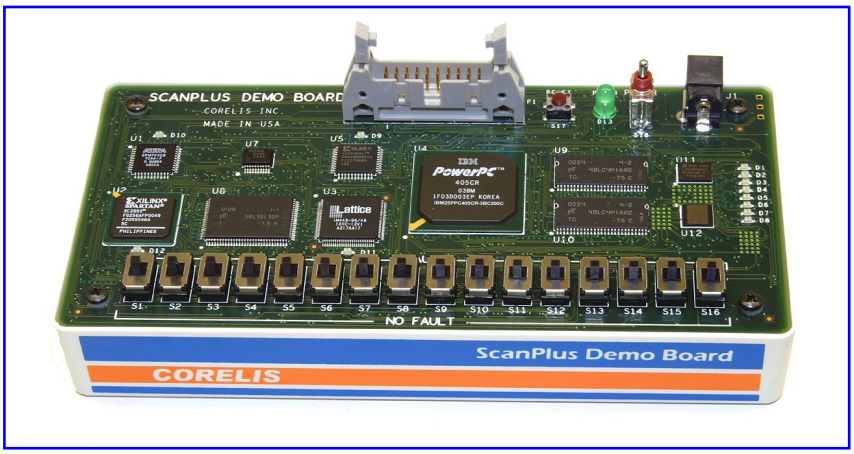
ScanPlus Demo Board™

Boundary-Scan Demonstration Board

- **Excellent tool for learning boundary-scan using the latest device technology**
- **Getting started tutorial using the ScanPlus Demo Board provided with each of the ScanPlus software products**
- **PowerPC 405 based system**
- **1 Mb (32K x 32) SSRAM**
- **64Mb (4M x 16) SDRAM (x2)**
- **4Mb AM29LV400 (256K x 16) FLASH (for in system FLASH programming)**
- **16MB 28F160B3 (1M x 16) FLASH (for in system FLASH programming)**
- **ISP supported for the following CPLD devices:**

  Altera 7032B
  Lattice Mach 4A3
  Xilinx 9536XL

- **User Programmable Xilinx FPGA**
- **16 Fault Insertion Switches allow the demonstration of a wide variety of fault conditions**
- **TAP header for easy connection to any Corelis boundary-scan controller**
- **Multi-layer, low noise PCB construction with ground and power planes**
- **Supplied software contains BSDL and other files for automatic test pattern generation along with schematic in PDF**
- **Fully compatible with ScanPlus family of products for testing and in-system programming of Flash memories and CPLDs**



Overview

The ScanPlus Demo Board was created to help ScanPlus user's gain the highest possible level of boundary-scan expertise in the shortest possible time frame. By using the ScanPlus Demo Board, a user is able to create actual test steps and execute them on physical hardware, insert faults, and observe diagnostic displays. Step by step instructions are provided that detail both the operation and rationale behind each test sequence.

The user's manuals for each of the ScanPlus products utilize the ScanPlus Demo Board to provide specific examples of how to use the various tools. By reading through the material and executing the example test plans, the user can gain a concrete understanding of each of the various boundary-scan concepts and ScanPlus products.

The ScanPlus Demo Board contains a variety of the latest components and package types, including fine pitch BGA packaging, that offers a tremendous challenge to traditional testing. Working through the detailed documentation and performing the operations on the actual hardware will allow both new and experienced boundary-scan users to gain considerable proficiency with the latest techniques in boundary-scan testing and in-system programming with very little time and effort.

General Description

The ScanPlus Demo Board is a high performance single board computer system that is based on the IBM PowerPC 405CR 32-bit RISC Embedded Controller. It was created to test and demonstrate complex boundary-scan applications such as interconnect testing, cluster testing, memory testing, in circuit emulation, in system programming (ISP) and Flash programming. The ScanPlus Demo Board has 16 switches that insert faults for demonstration of boundary-scan testing and diagnosis.

Features

The ScanPlus Demo Board includes the following boundary-scan devices in its scan chain:

U1 – Altera 7032B CPLD

U2 – Xilinx Spartan FPGA

U3 – Lattice Mach 4A3 CPLD

U4 – IBM PowerPC 405CR

U5 – Xilinx 9536XL CPLD

The ScanPlus Demo Board also features the following peripheral devices that may be tested via boundary-scan:

U7 – 74LVC244 Buffer

U8 – Micron SSRAM Memory (32K x32)

U9 – Micron SDRAM Memory (4M x 16)

U10 – Micron SDRAM Memory (4M x 16)

U11 – AMD Flash (256K x 16)

U12 – Intel Flash (1M x 16)

Fault Insertion Switches

Fault insertion switches have been provided to demonstrate fault detection and diagnostics during boundary-scan testing.

Boundary-Scan TAP

The ScanPlus Demo Board is equipped with a Boundary-Scan Test Access Port (TAP) that is compliant with IEEE-1149.1 standards. Boundary-scan and ISP tools access the ScanPlus Demo Board TAP through the 20-pin connector P1. The Corelis boundary-scan controllers connect to P1 with a 20-pin 1:1 flat cable. Table 1 shows the connection list for P1.

Pin	SIGNAL Name	I/O	Description
1	TRST*	In	Test Logic Reset
3	TDI	In	Test Data In to the ScanPlus Demo Board, Test Data Out from the controller
5	TDO	Out	Test Data Out from the ScanPlus Demo Board, Test Data In to the controller
7	TMS	In	Test Mode Select
9	TCK	In	Test Clock
11	Write_Strobe*	In	Active Low External Write Strobe for Flash Programming
13	GPIO2	In	Used to Remotely Turn Board Power On
15	Ready/Busy*	Out	Active Low Ready/Busy Signal for Flash Programming
17	2.5V		Used for power shorts test
18	-	-	Reserved (Do Not Connect)
19	3.3V		Used for power shorts test

Table 1. JTAG Connector P1 Pin Assignment

Note: Even pins are ground

CORELIS

13100 Alondra Blvd.
Cerritos, California 90703
Tel: (562) 926-6727, Fax: (562) 404-6196
sales@corelis.com www.corelis.com