

Using JTAG Emulation for Board-Level Functional Test

Demanding Test Requirements for Processor Based Boards

As chip packaging and interconnectivity have become more dense and operate at higher clock frequencies, physical access for traditional bed-of-nails testing becomes limited. This results in loss of ICT (in-circuit test) fault coverage and higher test fixture costs. Reduced fault coverage, coupled with limited diagnostic resolution at ICT and FT (functional test), often add up to excessive debug times at ICT/FT repair stations. These costly, extended repair cycles can severely hamper, if not prevent, effective manufacture of processor based PCBs (printed circuit boards). Compounding the challenges manufacturers now have to face is the fact that traditional test and inspection solutions no longer provide the capability of verifying the complete integrity of the soldering process. For example, X-ray inspection is not reliable for detecting cold solder joints.

Also, during the product development process, board designers are confronted with a more complex tree-like structure, involving a tighter integration between hardware and software for processor based boards. So, when limited test access and complex product design combine to make test methods more costly and less effective, is there a reliable solution? With Corelis' ScanExpress JTAG Embedded Test (JET) solution, there is.

What is JET and how does it work? JTAG Emulation is the key.

In the 80's and 90's, In-Circuit Emulation (ICE) was a popular approach for processor based boards. However, its decline was driven by the absence of socketed processors and ROM devices in new designs. With the advent of JTAG (Joint Test Action Group) and the resulting IEEE 1149.1 standard, most processors have incorporated a test protocol port. While primarily born out of the need to overcome test access problems of fine-pitch components including BGAs, the JTAG port now offers the ability to access internal registers and memories, as well as the ability to apply breakpoints, similar to the emulators of the past, but without being obtrusive, slowing the processor, or requiring target system hardware or software resources. JTAG provides all of the capabilities of a debugger while offering the potential for functional testing of a unit-under-test (UUT) at full operating speed. JTAG also opens up the possibility of marrying boundary-scan based structural testing with functional testing as a straightforward alternative or extension to a test strategy based solely on ICT.

Simply stated, boards with bus architecture allow on-board emulation to take over control via one of the buses. This allows emulation to take full control over all of the processor buses.

The result is a debug interface port which offers synergic benefits up-stream (board design) and down-stream (board test). These benefits enable users to exploit JTAG to enhance structural and functional test coverage potential for boundary-scan as well as non-boundary-scan devices.

So, how is the potential realized? By employing a unique hybrid approach, combining the benefits of boundary-scan and JTAG functional testing into a single software package called, ScanExpress JET.

Enhancing Boundary-Scan with JTAG Embedded Test

Corelis' ScanExpress JET represents a major step forward for automatic circuit board testing. The JTAG Embedded Test method extends coverage beyond popular boundary-scan techniques to virtually every signal of the UUT that is accessible by the on-board CPU(s). This includes most of the remaining non-scannable, analog, and I/O port resources. As a bonus, it employs full-speed functionality verification without modifications to the circuit, its onboard firmware, or the test fixture.

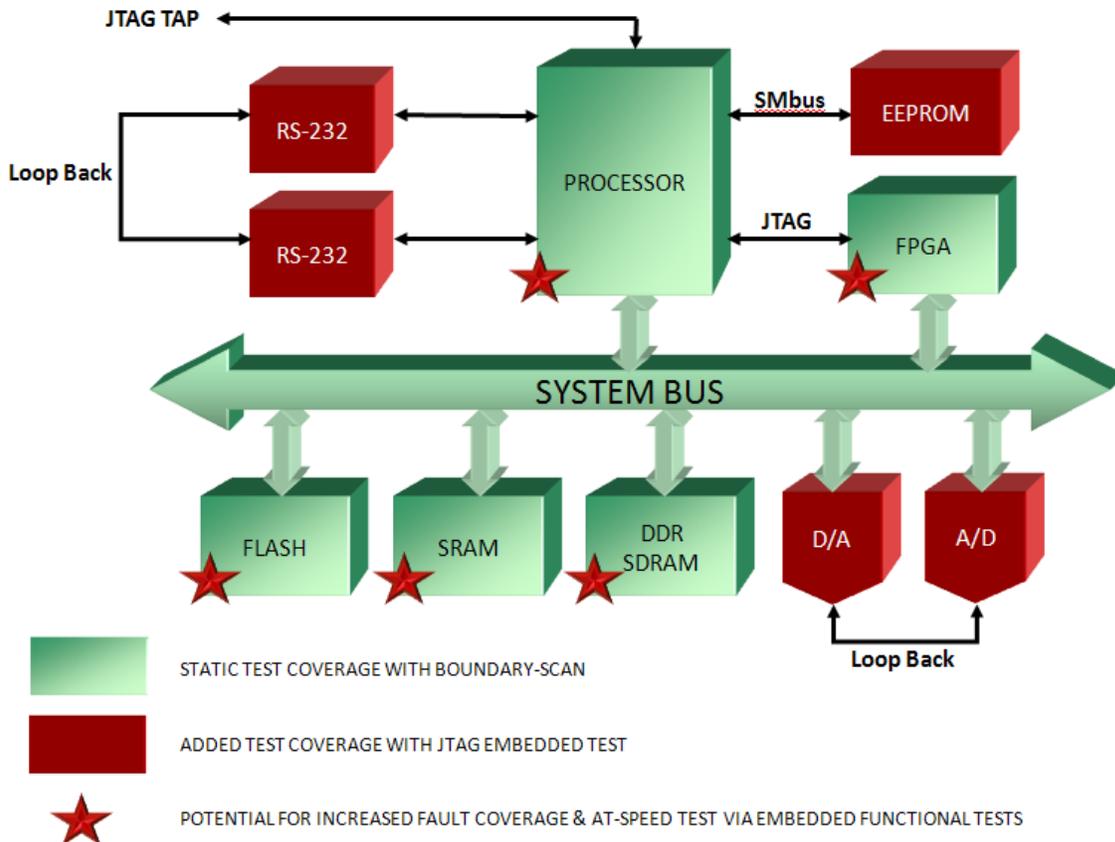


Figure 1 – Combining Boundary-Scan and JTAG Embedded Test for Increased Test Coverage and At-Speed Functional Test Benefits

Connecting to the UUT

As shown in Figure 1, a board may include a single JTAG TAP (Test Access Port) that is dedicated to a specific CPU. This TAP is used for software debug and boundary-scan test. A board may also include multiple JTAG TAPs (not shown here), with one of them being used for software debug and boundary-scan test, and the other TAPs used for boundary-scan test. Corelis' JTAG controllers support multiple TAP configurations under a single controller. There is no need to switch cables or use relays when moving from a debug to test environment or switching from boundary-scan test to functional test. ScanExpress JET comes with a comprehensive device library and utilities so boundary-scan and functional test development times are significantly shortened.

ScanExpress JET Benefits

ScanExpress JET can be used either as a stand-alone test technique or to augment existing boundary-scan capabilities. It is relatively inexpensive to deploy, especially when supplementing boundary-scan testing already in use. Because board access is through the JTAG port, ScanExpress JET may be usable even when a board is not able to boot to its full functionality. It automatically generates exhaustive tests for many different kinds of memories and other peripherals. The benefits of ScanExpress JET include:

- Improved test coverage and fault diagnostics
- One test station and GUI for boundary-scan (structural) test, functional at-speed test, and in-system programming (ISP)
- Dramatic reduction in the time it takes to develop functional tests
- Reduced use of ICTs
- Fast device programming
- “Dead” board debug
- Complete interactive control/visibility of the UUT resources

These benefits are applicable in both the development and production phases. During development, the board bring-up engineer can deliver fully proven at-speed functionality to the software integration/debug team with confidence. The code validation team can focus entirely on the application, without fighting undiscovered board snags. The JET method, in most cases, allows testing without the need to write a single line of special bring-up debug code.

While ScanExpress JET is primarily intended to aid test coverage during the manufacturing phase of circuit boards, its deployment yields significant assistance across the entire product life-cycle. ScanExpress JET is beneficial for:

- Test engineers that want a low cost alternative to augment ICT test coverage and extend boundary-scan testing with at-speed functional testing
- Design engineers that need to debug prototype boards at-speed before embedded firmware and test fixtures are available
- Embedded firmware and software engineers that want to save time and resources by creating diagnostics tests automatically
- Field application engineers that want to perform a quick on-site validation of a customer’s board or update product firmware in the field
- Repair station engineers who want to find board failures quickly and reduce the amount of debug effort

With ScanExpress JET, test developers do not need to be aware of the product application behavior, nor is any software programming ability required. ScanExpress JET has all the required target circuit board knowledge built-in. However, it remains extensible should the user wish to add customized user code. Table-1 depicts how combining the features of boundary-scan test with JET increases the test coverage, reduces test development, and lowers test cost for a relevant PCB.

Feature	Boundary-Scan	JTAG Embedded Test	Boundary-Scan and JTAG Embedded Tests
Structural coverage	Very good	Good	Excellent
Functional coverage	Low	High	High
Programming speed	Average	Excellent	Excellent
Test time	Fast	Fast	Fast
Test points required	Few	Few	Very Few
Test development	Automatic	Semi-auto	Auto/Semi
Diagnostics	Excellent	Average	Excellent

Table-1 Combining Boundary-Scan and JTAG Embedded Test to Increase Test Coverage

To better appreciate the advantages of ScanExpress JET, Table-2 outlines the quantitative advantages in further detail. The most popular system for electrical process test is the ICT. The average capital cost for a basic ICT is US \$125,000. A fixture kit will start at approximately US \$5,000. But, depending upon the size and complexity, a finished fixture could cost more than US \$15,000. The high fixture cost will be driven by the node-count of the board. Typically, processor based boards have high node counts and are further compounded by fine line pitch multi-layer boards and BGA type devices. The reduction in ICT fixture cost is quite dramatic when test fixture complexity is minimized by accessing digital nodes with a combination of boundary-scan and JET.

Due to the high initial cost of ICTs, combining or replacing ICT with boundary-scan and JET testing can provide tremendous cost saving. The incremental investment over adding boundary-scan and JET is easily justified because of the substantial savings in both fixture cost and test development time. The savings become even more evident as board complexity increases.

Obviously, one must factor in the mix of devices, technologies, board sizes, and overall node count. But, all things considered, boundary-scan and JTAG Embedded Test are solutions that merit strong consideration for processor based board designs in the manufacturing environment.

	ICT	Adding Boundary-Scan	Adding JET	Adding Boundary-Scan and JET
Average acquisition cost (\$ US)	\$\$\$\$\$	\$\$	\$	\$\$\$
Average ICT Fixture cost	\$\$\$	\$\$	\$	\$
Test development cost	\$\$\$	\$	\$	\$
Test throughput (cost per sec.)	\$\$\$	\$\$	\$	\$
Coverage cost	\$\$\$\$	\$\$	\$\$	\$

Table-2 Quantitative Cost Improvements with Boundary-Scan and Embedded Test

Technical Elements Combine for an Advantageous Test Synergy

ScanExpress JET provides customers with an integrated development and execution test environment, combined with a single point of contact and support. The JET testing method depends on the UUT having a JTAG-enabled CPU on-board. The JTAG Test Access Port (TAP) is generally routed to a single emulation connector on the board. Other JTAG interconnect scan-chains may be connected to a different JTAG connector to be used during boundary-scan testing. The CPU debug TAP brings control and visibility of the processor itself to the host. This is the same TAP employed by JTAG emulators for software development and debug, with the resulting access to the CPU register/control structures, attached memory, and the ability to utilize the CPU debug running/stepping facilities for testing. The JET method harnesses the power of the target's embedded CPU to assist in the code download, device programming, and testing operations – all at full processing speed. CPU's that include a JTAG debug port typically perform the following operations:

- Run
- Stop
- Step
- Write to Registers and memory
- Read from Registers and memory
- Exchange parameters with the JTAG host
- Display CPU status

The host software uses these features to download test/diagnostics routines into the CPU's cache memory and into the target memory. These routines execute at-speed and pass the test results to the host. There is no need to modify the on-board application software, typically stored in Flash memory. Indeed, the Flash itself can be similarly programmed using the CPU as an algorithm expediter. This avoids the slower "wiggling" approach of JTAG flash programming.

In Conclusion

Employing JET and boundary-scan testing provides a useful tool that brings together two independent test technologies, boundary-scan with functional at-speed testing. With new processor debug interfaces that support JTAG and thus the ability to bypass the board's normal operating software, functional test times can be slashed from minutes to seconds. Additionally, boundary-scan structural tests can be executed in advance of functional tests, providing more detailed resolution during fault detection.

About Corelis

Corelis, Inc., a subsidiary of EWA Technologies, Inc., offers the industry's broadest line of boundary-scan software and hardware products that combine exceptional ease-of-use with advanced technical innovation and unmatched customer service. Corelis' ScanExpress Boundary-Scan systems are used for interconnect testing and In-System Programming (ISP) of Flash memories, CPLDs, and FPGAs. Systems include a complete range of IEEE-1149.1 compatible boundary-scan controllers for PCI, PC-Card, Ethernet, USB 2.0, cPCI/cPXI, and VXI host interfaces. Corelis also provides custom test engineering services, including test procedure development and integration. For more information about Corelis, please visit www.corelis.com