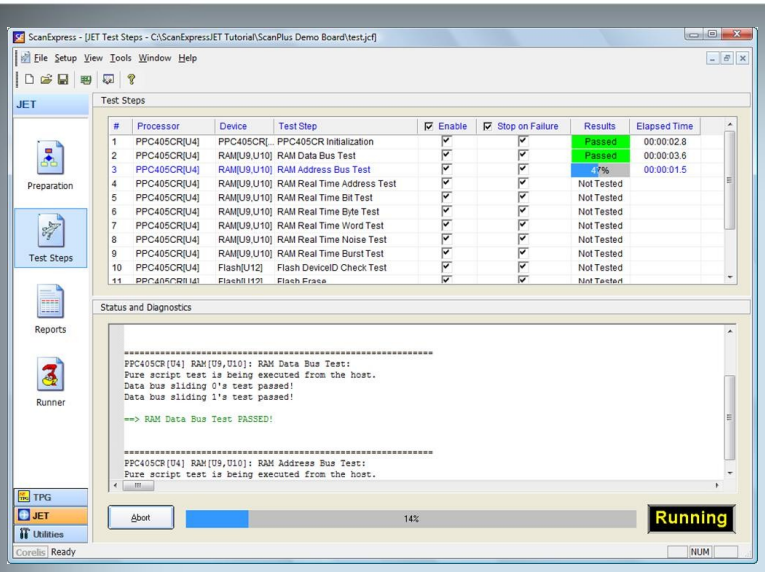
# ScanExpress JET™

## At-Speed Non-Intrusive Functional Testing

CORELIS An EWA Company

*Preferred Functional Test Solutions—Acclaimed Technical Support*




Functional circuit board testing presents many challenges that are often costly and time consuming. Most functional tests need to be customized for each design, limiting reusability. This results in software engineers vying for time between development code and test code. Even when functional tests become available, the diagnostic details are often inadequate to give clear visibility on a given problem.

ScanExpress JET is a tool designed to overcome these challenges by automating the functional test generation process on CPU–based IEEE-1149.1 compliant circuit boards. Coined *JTAG Embedded Test*, JET is the preferred method for at-speed, non-intrusive functional testing.

### Features

- ❑ Dramatically enhances UUT test coverage when it includes a CPU with a JTAG debug/emulation port
- ❑ CPU assists at-speed testing using test routines downloaded via JTAG into CPU cache memory or external RAM
- ❑ JTAG Embedded Tests are able to be combined with boundary-scan structural tests for extended test coverage
- ❑ Automatic generation of functional tests for common peripherals
- ❑ Software guides the user through a logical sequence of steps for constructing test steps from start to finish
- ❑ "C"-style command file script language with single-step capability assists in writing custom test sequences
- ❑ Extends coverage beyond boundary-scan for:
  - All CPU accessible resources
  - Boundary-scan inaccessible components and analog devices
  - I/O port testing using external equipment
- ❑ In-System Programming (ISP) of Flash up to theoretical speeds
- ❑ Large library of supported processors
- ❑ Automatically constructs test plans for integration into the ScanExpress Runner™ test execution sequencer (sold separately)

### Benefits

- Improves test coverage and fault diagnostics
- Dramatically reduces the time it takes to develop functional tests
- Reduces ICT usage and related fixture costs
- Programs devices up to theoretical speeds
- Helps identify why boards don't boot
- Helps detect hard to find power and ground structural defects

### Applications

- **Test Engineers** - JET is able to increase board test coverage by quickly combining boundary-scan testing with at-speed functional testing.
- **Design Engineers** - JET assists in prototype debug before test firmware or test fixtures are available
- **Firmware/Software Engineers** - JET is able to save coding time through automatic test and diagnostic generation.
- **Field Application Engineers** - JET can be used to field validate a customer board or upgrade firmware on-site.
- **Repair Engineers** - JET can identify board failures quickly reducing the repair cost per unit.

***Learn More:*** For more information about Corelis products, please visit **www.corelis.com**

# ScanExpress JET™

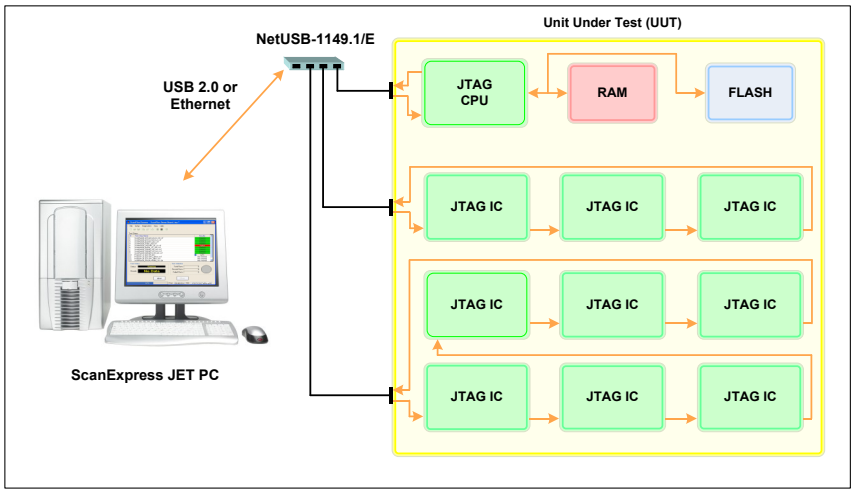
JET automates at-speed functional test development of peripheral components that interface with an IEEE-1149.1 compatible CPU. JET provides a peripheral component library that allows reusability across multiple CPU platforms. The highly customizable diagnostic scripts provide users with the pinpoint resolution they need to clearly identify failures. Corelis offers both a stand-alone JET solution as well as a combined solution with traditional JTAG structural interconnect testing. JET is ideal for testing boards without the need to modify the PCB circuitry or the on-board firmware. JET operates through a CPU's JTAG port to provide users simplified access to the following operations:

- Run, Stop, and Step Functions
- Ability to Write to Registers and Memory
- Ability to Read from Registers and Memory
- Exchange Parameters with the JTAG Host
- Display CPU Status

The host software automatically uses these features to download test & diagnostic routines into the CPU's cache or external memory. These routines then execute at full processor speed and send results back to the host.

| Feature | Boundary-Scan Test | Functional Test | Combined Test |
|---|---|---|---|
| Structural coverage | Very good | Good | Excellent |
| Functional coverage | Low | High | High |
| Programming (ISP) time | Average | Excellent | Excellent |
| Test time | Fast | Fast | Fast |
| Test points required | Very few | Very few | Very few |
| Test development | Automatic | Semi Auto | Automatic |
| Diagnostics | Excellent | Average | Excellent |

**Combining JTAG and Functional Test to Increase Test Coverage**




**UUT configuration combining a single CPU scan-chain with two additional scan chains using a NetUSB-1149.1/E controller**

## Connecting to a UUT

JET requires a UUT with a JTAG-enabled processor having external access to its Test Access Port (TAP). A Corelis controller serves as the interface between the PC and the TAP interface.

Boards typically include a single JTAG TAP connector that is dedicated to the CPU. This TAP is often used for JTAG–based software debug and emulation. Boards may also include other JTAG TAP connectors, primarily being used for boundary-scan test and in-system programming.

The figure above depicts connecting a Corelis NetUSB-1149.1/E™ four-port JTAG controller to a board that includes three separate TAP connectors: a CPU with a dedicated JTAG port, and two additional JTAG ports containing other boundary-scan compatible devices.

The ScanExpress JET system is also able to handle cases where the CPU and other boundary-scan devices share the same scan-chain.

## Ordering Information

### Part Number - 20700

- ScanExpress JET Test Development System supporting both Test Program Generation and Execution.

### Part Number - 207XX

- CPU specific support package for ScanExpress JET. Contact Corelis for a list of supported processors and part numbers.

**Note: At least one CPU support package must be purchased with the ScanExpress JET Test Development System.**

For more information about this product, view the ScanExpress JET whitepaper on our website:

http://www.corelis.com/whitepapers/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