Boundary-Scan for PCB Interconnect Testing
and In-System Programming of CPLDs and Flash Memories

.Introduction

Since its introduction as an industry standard in 1990, boundary-scan – also known as JTAG – has enjoyed growing popularity for board level manufacturing test applications. Boundary-scan has rapidly become the technology of choice for building reliable high technology electronic products with a high degree of testability. Due to the low-cost and IC level access capabilities of boundary-scan, its use has expanded beyond traditional board test applications into product design and service.

This article provides a brief overview of the boundary-scan architecture and the new technology trends that make using boundary-scan essential for dramatically reducing development and production costs, speeding test development through automation, and improving product quality because of increased fault coverage. The article also describes the various uses of boundary-scan and the tools available today for supporting boundary-scan technology.

What is boundary-scan?

Boundary-scan, as defined by the IEEE Std.-1149.1 standard, is an integrated method for testing interconnects on printed circuit boards (PCBs) that are implemented at the integrated circuit (IC) level. The inability to test highly complex and dense printed circuit boards using traditional in-circuit testers and bed of nail fixtures was already evident in the mid eighties. Due to physical space constraints and loss of physical access to fine pitch components and BGA devices, fixturing cost increased dramatically while fixture reliability decreased at the same time.

A brief history of boundary-scan

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was standardized in 1990 as the IEEE Std. 1149.1-1990. In 1993 a new revision to the IEEE Std. 1149.1 standard was introduced (titled 1149.1a) and it contained many clarifications, corrections, and enhancements. In 1994, a supplement containing a description of the Boundary-Scan Description Language (BSDL) was added to the standard. Since that time, this standard has been adopted by major electronics companies all over the world. Applications are found in high volume, high-end consumer products, telecommunication products, defense systems, computers, peripherals, and avionics. In fact, due to its economic advantages, some smaller companies that cannot afford expensive in-circuit testers are using boundary-scan.

Figure 1. Typical boundary-scan cell

The boundary-scan test architecture provides a means to test interconnects between integrated circuits on a board without using physical test probes. It adds a boundary-scan cell that includes a multiplexer and latches to each pin on the device. Boundary-scan cells in a device can capture data from pin or core logic signals, or force data onto pins. Captured data is serially shifted out and externally compared to the expected results. Forced test data is serially shifted into the boundary-scan cells. All of this is controlled from a serial data path called the scan path or scan chain. Figure 1 depicts the main elements of a boundary-scan device. By allowing direct access to nets, boundary-scan eliminates the need for a large number of test vectors, which are normally needed to properly initialize sequential logic. Tens or hundreds of vectors may do the job that had previously required thousands of vectors. Potential benefits realized from the use of boundary-scan are shorter test times, higher test coverage, increased diagnostic capability and lower capital equipment cost.

The principles of interconnect test using boundary-scan are illustrated in Figure 2. Figure 2 depicts two boundary-scan compliant devices, U1 and U2, which are connected with four nets. U1 includes four outputs that are driving the four inputs of U2 with various values. In this case, we assume that the circuit includes two faults: a short between Nets 2 and 3, and an open on Net 4. We will also assume that a short between two nets behaves as a wired-AND and an open is sensed as logic 1. To detect and isolate the above defects, the tester is shifting into the U1 boundary-scan register the patterns shown in Figure 2 and applying these patterns to the inputs of U2. The inputs values of U2 boundary-scan register are shifted out and compared to the expected results. In this case, the
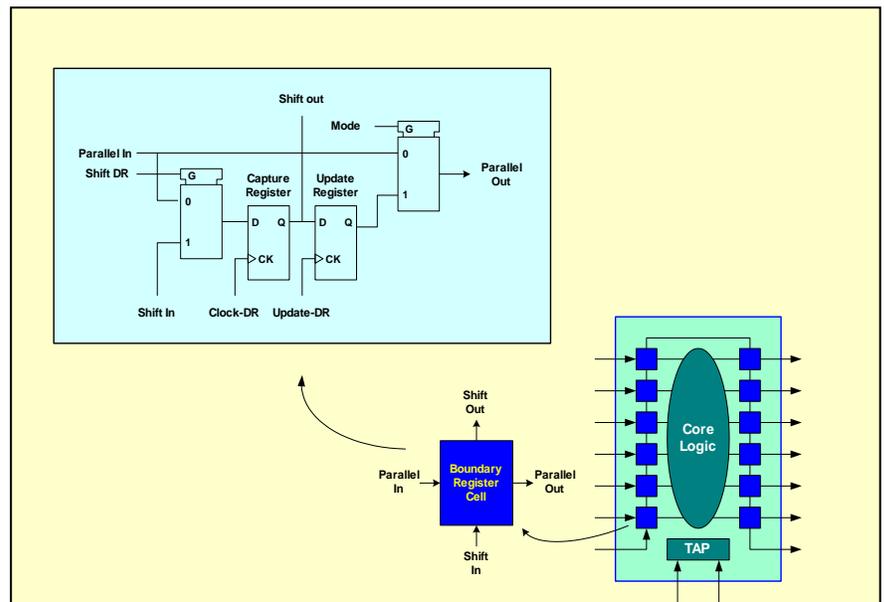
results (marked in red) on Nets 2, 3, and 4 do not match the expected values and, therefore, the tester detects the faults on Nets 2, 3, and 4.

Boundary-scan tool vendors provide various types of stimulus and sophisticated algorithms, not only to detect the failing nets, but also to isolate the faults to specific nets, devices, and pins.

Boundary-scan applications

While it is obvious that boundary-scan based testing can be used in the production phase of a product, new developments and applications of the IEEE-1149.1 standard have enabled the use of boundary-scan in many other product life cycle phases. Specifically, boundary-scan technology is now applied to product design, prototype debugging and field service as depicted in Figure 3. This means the cost of the boundary-scan tools can be amortized over the entire product life cycle, not just the production phase.

To facilitate this product life cycle concept, boundary-scan tool vendors such as Corelis offer an integrated family of software and hardware solutions for all phases of a product's life-cycle. All of these products are compatible with each other, thus protecting the user's investment.

Applying boundary-scan for product development

The ongoing marketing drive for reduced product size, such as portable phones and digital cameras, higher functional integration, faster clock rates, and shorter product life-cycle with dramatically faster time-to- market has created new technology trends. These trends include increased device complexity, fine pitch components, such as surface-mount technology (SMT), systems-in-package (SIPs), multi-chip modules (MCMs), ball-grid arrays (BGAs), increased IC pin-count, and smaller PCB traces. These technology advances, in turn, create problems in PCB development:

❑ Many boards include components that are assembled on both sides of the board. Most of the through-holes and traces are buried and inaccessible.

❑ Loss of physical access to fine pitch components, such as SMTs and BGAs, makes it difficult to probe the pins and distinguish between manufacturing and design problems.

❑ Often a prototype board is hurriedly built by a small assembly shop with lower quality control as compared to a production house. A prototype generally will include more assembly defects than a production unit.

❑ When the prototype arrives, a test fixture for the ICT is not available and, therefore, manufacturing defects cannot be easily detected and isolated.

❑ Small-size products do not have test points, making it difficult or impossible to probe suspected nodes.

❑ Many Complex Programmable Logic Devices (CPLDs) and flash memory devices (in BGA packages) are not socketed and are soldered directly to the board.

❑ Every time a new processor or a different flash device is selected, the engineer has to learn from scratch how to program the flash memory.

❑ When a design includes CPLDs from different vendors, the engineer must use different in-circuit programmers to program the CPLDs.
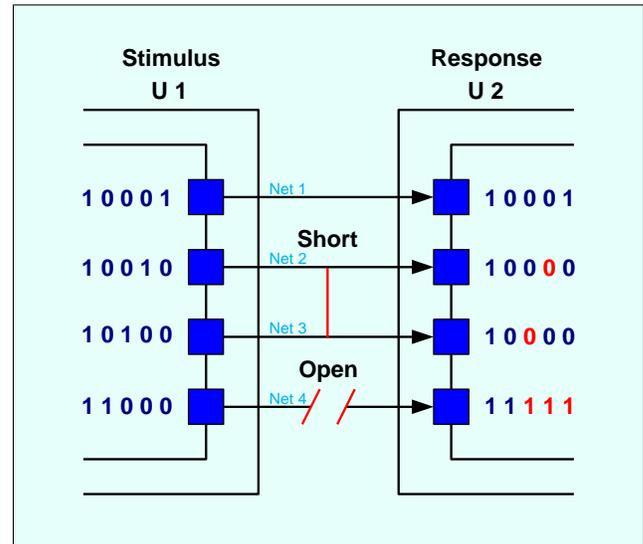
Boundary-scan technology is the only cost-effective solution that can deal with the above problems. In recent years, the number of devices

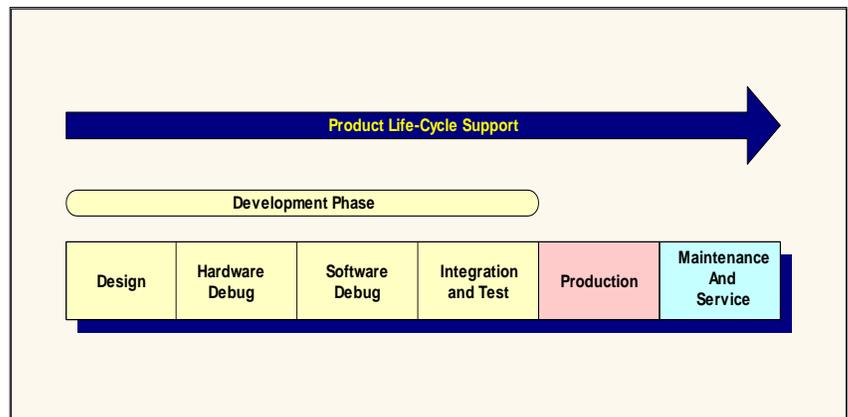**Figure 2. Interconnect test example**

Figure 3. Product life cycle support

that include boundary-scan has grown dramatically. Almost every new microprocessor that is being introduced includes boundary-scan circuitry for testing and in-circuit emulation. Most of the CPLD and field programmable array (FPGA) manufacturers, such as Altera, Lattice and Xilinx, to mention a few, have incorporated boundary-scan logic into their components, including additional circuitry that uses the boundary-scan four-wire interface to program their devices in-system.

As the acceptance of boundary-scan as the main technology for interconnect testing and in-system programming (ISP) has increased, the various boundary-scan test and ISP tools have matured as well. The increased number of boundary-scan components and mature boundary-scan tools, as well as other factors that will be described later, provide engineers with the following benefits:

❑ Easy to implement Design-For- Testability (DFT) rules. A list of basic DFT rules is provided later in this article.

❑ Design analysis prior to PCB layout to improve testability.

❑ Packaging problems are found prior to PCB layout.

❑ Little need for test points.

❑ No need for test fixtures.

❑ More control over the test process.

❑ Quick diagnosis (with high resolution) of interconnection problems without writing any functional test code.

❑ Program code in flash devices.

❑ Design configuration data placement into CPLDs.

❑ JTAG emulation and source-level debugging.

What boundary-scan tools are needed?

In the previous section, we listed many of the benefits that a designer enjoys when incorporating boundary-scan in his product development. In this section we describe the tools and design data needed to develop boundary-scan test procedures and patterns for ISP, followed by a description of how to test and program a board. We use a typical board as an illustration for the various boundary-scan test functions needed. A block diagram of such a board is depicted in Figure 4.

A typical digital board with boundary-scan devices includes the following main components:

❑ Various boundary-scan components, such as CPLDs, FPGAs, processors, etc., chained together via the boundary-scan path.

❑ Non-boundary-scan components (clusters).

❑ Various types of memory devices.

❑ Flash memory components.

❑ "Transparent" components, such as series resistors or buffers.

Most of the boundary-scan test systems are comprised of two basic elements: Test Program Generation and Test Execution. Generally, a Test Program Generator (TPG) requires the netlist of the Unit Under Test (UUT) and the BSDL files of the boundary-scan components. The TPG automatically generates test patterns that allow fault detection and isolation for all boundary-scan testable nets of the PCB. A good TPG can be used to create a thorough test pattern for a wide range of designs. For example, ScanExpressTPG typically achieves net coverage of more than 60%, even though the majority of the PCB designs are not optimized for boundary-scan testing. The TPG also creates test vectors to detect faults on the pins of non-scannable components, such as clusters and memories that are surrounded by scannable devices.
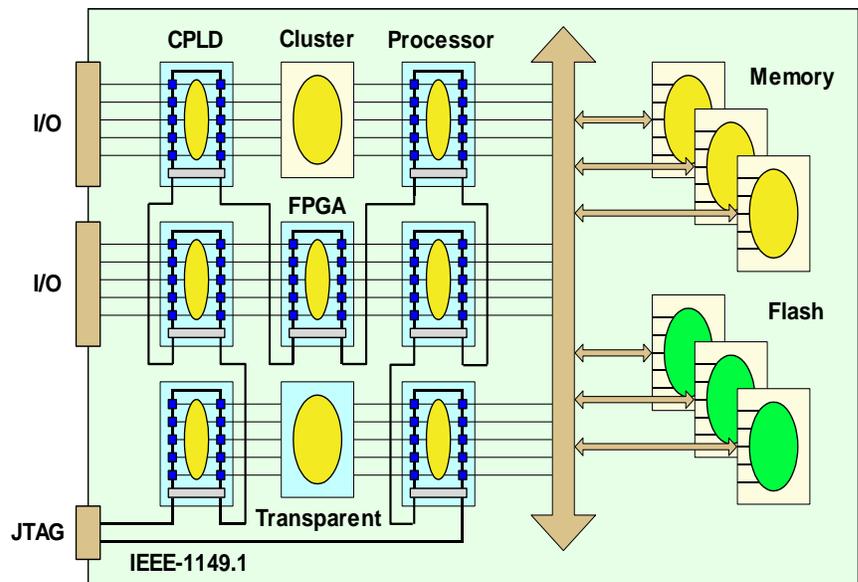

Figure 4. Typical board with boundary-scan components

Some TPGs also generate a test coverage report that allows the user to focus on the non-testable nets and determine what additional means are needed to increase the test coverage.

Test programs are generated in seconds. For example, when Corelis ScanExpressTPG™ was used, it took a 3.0 GHz Pentium 4 PC 23 seconds to generate an interconnect test for a UUT with 5,638 nets (with 19,910 pins). This generation time includes netlist and all other input files processing as well as test pattern file generation.

Test execution tools from various vendors provide means for executing boundary-scan tests and performing in-system programming in a pre-planned specific order, called a test plan. Test vectors files, which have been generated using the TPG, are automatically applied to the UUT and the results are compared to the expected values. In case of a detected fault, the system diagnoses the fault and lists the failures as depicted in Figure 5. Figure 5 shows the main window of the Corelis test execution tool, ScanExpress Runner™. ScanExpress Runner gives the user an overview of all test steps and the results of executed tests. These results are displayed both for individual tests as well as for the total test runs executed. ScanExpress Runner provides the ability to add or delete various test steps from a test plan, or re-arrange the order of the test steps in a plan. Tests can also be enabled or disabled and the test execution can be
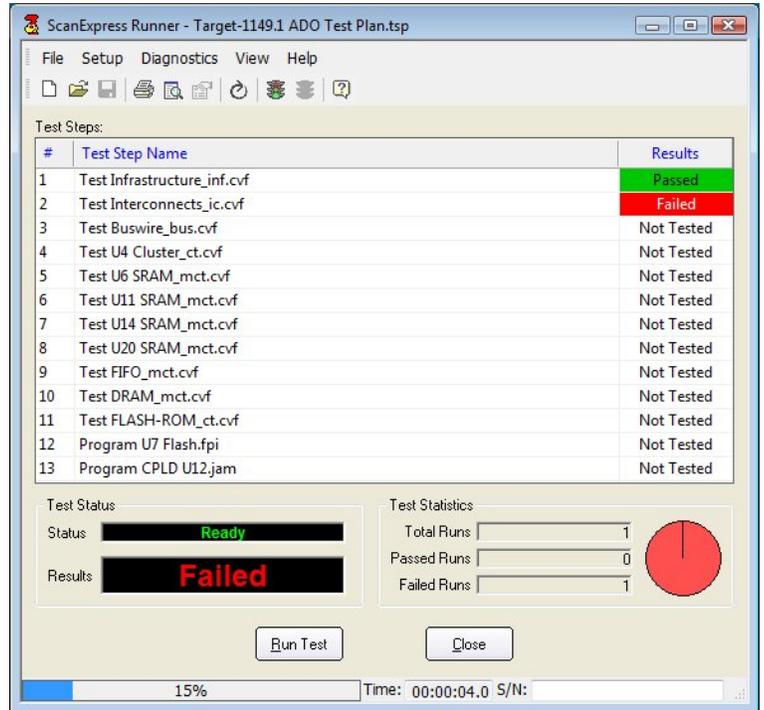

Figure 5. ScanExpress Runner main window

stopped upon the failure of any particular test.

Different test plans may be constructed for different UUTs. Tests within a test plan may be re-ordered, enabled or disabled, and unlimited different tests can be combined into a test plan. ScanExpress Runner can be used to develop a test sequence or test plan from various independent sub-tests. These sub-tests can then be executed sequentially as many times as specified or continuously if desired. A sub-test can also program CPLDs and flash memories. For ISP, other formats, such as SVF, JAM, and STAPL, are also supported.

To test the board depicted in Figure 4, the user must execute a test plan that consists of various test steps as shown in Figure 5. The first and most important test is the scan chain infrastructure integrity test. The scan chain must work correctly prior to proceeding to other tests and ISP. Following a successful test of the scan chain, the user can proceed to testing all the interconnections between the boundary-scan components. If the interconnect test fails, ScanExpress Runner displays a diagnostic screen that identifies the type of failure (such as stuck-at, Bridge, Open) and lists the failing nets and pins as shown in Figure 6. Once the interconnect test passes, including the testing of transparent components, it makes sense to continue testing the clusters and the memory devices. At this stage, the system is ready for in-system programming, which typically takes more time as compared to testing.

During the design phase of a product, some boundary-scan vendors will provide design assistance in selecting boundary-scan-compliant components, work with the
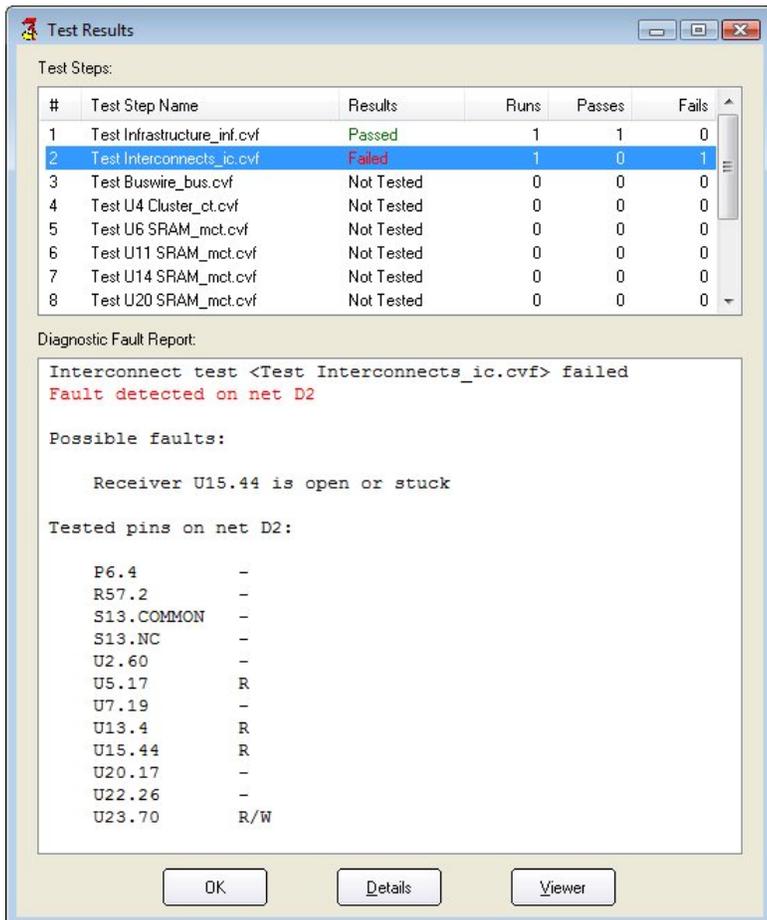

Figure 6. Diagnostics display

developers to ensure that the proper BSDL files are used, and provide advice in designing the product for testability.

Applying boundary-scan at production test

Production testing, when utilizing traditional in-circuit testers that do not have boundary-scan features installed, suffers from similar problems that product developers have and more:

- Loss of physical access to fine pitch components, such as SMTs and BGAs, reduces bed-of-nails ICT fault isolation.
- Development of test fixtures for ICTs becomes longer and more expensive.
- Development of test procedures for ICTs becomes longer and more expensive due to more complex ICs.
- Designers are forced to bring out a large number of test points, which is in direct conflict with the goal to miniaturize the design.
- In-system programming is inherently slow, inefficient, and expensive if done with an ICT.
- Assembling boards with BGAs is difficult and subject to numerous defects, such as solder smearing.

JTAG Embedded Functional Test

Recently, a test methodology has been developed which combines the ease-of-use and low cost of boundary-scan with the coverage and security of traditional functional testing. This new technique, called JTAG Embedded Test (JET), lets engineers automatically develop PCB functional test that can be run at full speed., If the PCB has an on-board processor with a JTAG port (common, even if the processor doesn't support boundary-scan), JET and boundary-scan tests can be executed as part of the same test plan to provide extended fault coverage to further complement or replace ICT testing.

Corelis ScanExpress JET™ provides JTAG embedded test for a wide range of processors. For more information about this technology and product, visit http://www.corelis.com/products/ScanExpressJET.htm.

Production test flow

Figure 7 shows different production flow configurations. The diagram shows two typical ways that boundary-scan is deployed:

- As a stand-alone application at a separate test station or test bench to test all the interconnects and perform ISP of on-board flash and other memories. JTAG embedded functional test (JET) may be integrated with boundary-scan.
- Integrated into the ICT system, where the JTAG control hardware is embedded in the ICT system and the boundary-scan (and possibly JET) software is a module called from the ICT software system.

In the first two cases, the test flow is sometimes augmented with a separate ICT stage after the JTAG-based testing is completed, although it is becoming more common for ICT to be skipped altogether or at least to be limited to analog or special purpose functional testing.

The following are major benefits in using boundary-scan test and ISP in production:

- No need for test fixtures.
- Integrates product development, production test, and device programming in one tool/system.
- Engineering test and programming data is reused in Production.
- Fast test procedure development.
- Preproduction testing can start the next day when prototype is released to production.
- Dramatically reduces inventory management – no pre-programmed parts eliminates device handling and ESD damage.
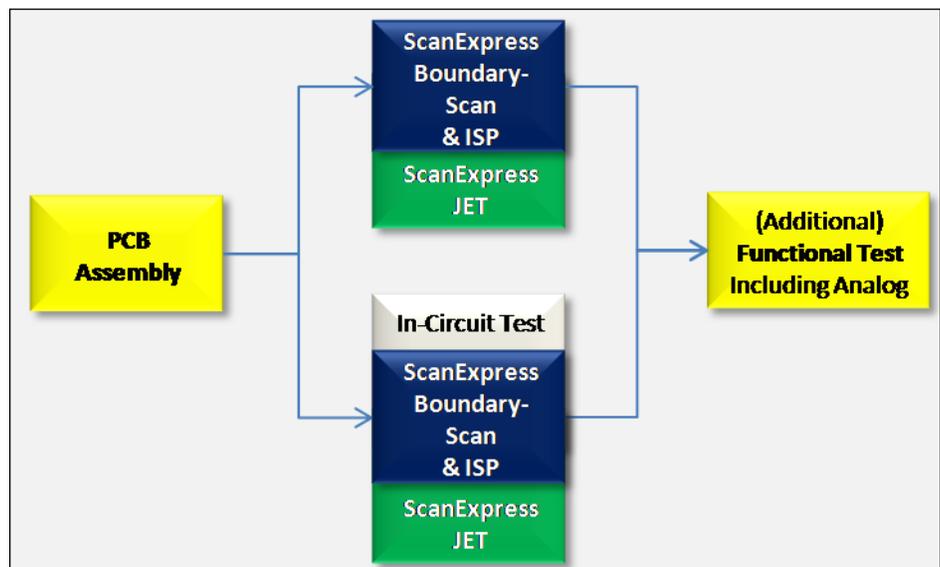- Eliminates or reduces ICT usage time – programming and screening.

Figure 7. Typical production flows

Production test is an obvious area in which the use of boundary-scan yields tremendous returns. Automatic test program generation and fault diagnostics using boundary-scan software products and the lack of expensive fixturing requirements can make the entire test process very economical. For products that contain edge connectors and digital interfaces that are not visible from the boundary-scan chain, boundary-scan vendors offer a family of boundary-scan controllable I/Os that provide a low cost alternative to expensive digital pin electronics.

Field service and installation

The role of boundary-scan does not end when a product ships. Periodic software and hardware updates can be performed remotely using the boundary-scan chain as a non-intrusive access mechanism. This allows flash updates and reprogramming of programmable logic, for example. Service centers that normally would not want to invest in special equipment to support a product now have an option of using a standard PC or laptop for boundary-scan testing. A simple PC-based boundary-scan controller can be used for all of the above tasks and also double as a fault diagnostic system, using the same test vectors that were developed during the design and production phase. This concept can be taken one step further by allowing an embedded processor access to the boundary-scan chain. This allows diagnostics and fault isolation to be performed by the embedded processor. The same diagnostic routines can be run as part of a power-on self-test procedure.

Boundary-scan design-for-test basic considerations

As mentioned earlier in this article, the design for boundary-scan test guidelines are simple to understand and follow compared to other traditional test requirements. It is important to remember that boundary-scan testing is most successful when the design and test engineering teams work together to ensure that testability is "designed in" from the start. The boundary-scan chain is the most critical part of boundary-scan implementations. When that is properly implemented, improved testability inevitably follows.

Below is a list of basic guidelines to observe when designing a boundary-scan-testable board:

❑ If there are programmable components in a chain, such as FPGAs, CPLDs, etc., group them together in the chain order and place the group at either end of the chain. It is recommended that you provide access to Test Data In (TDI) and Test Data Out (TDO) signals where the programmable group connects to the non-programmable devices.

❑ All parts in the boundary-scan chain should have 1149.1-compliant test access ports (TAPs).

❑ Use simple buffering for the Test Clock (TCK) and Test Mode Select (TMS) signals to simplify test considerations for the boundary-scan TAP. The TAP signals should be buffered to prevent clocking and drive problems.

❑ Group similar device families and have a single level converter interface between them, TCK, TMS, TDI, TDO, and system pins.

❑ TCK should be properly routed to prevent skew and noise problems.

❑ Use the standard JTAG connector on your board as depicted in Corelis documentation.

❑ Ensure that BSDL files are available for each boundary-scan component that is used on your board and that the files are validated.

Design for interconnect testing requires board-level system understanding to ensure higher test coverage and elimination of signal level conflicts.

❑ Determine which boundary-scan components are on the board. Change as many non-boundary-scan components to IEEE 1149.1-compliant devices as possible in order to maximize test coverage.

❑ Check non-boundary-scan devices on the board and design disabling methods for the outputs of those devices in order to prevent signal level conflicts. Connect the enable pins of the conflicting devices to boundary-scan controllable outputs. Corelis tools will keep the enable/disable outputs at a fixed disabling value during the entire test.

❑ Ensure that your memory devices are surrounded by boundary-scan components. This will allow you to use a test program generator, such as ScanExpressTPG, to test the interconnects of the memory devices.

❑ Check the access to the non-boundary-scan clusters. Make sure that the clusters are surrounded by boundary-scan components. By surrounding the non-boundary-scan clusters with boundary-scan devices, the clusters can then be tested using a boundary-scan test tool.

❑ If your design includes transparent components, such as series resistors or non-inverting buffers, your test coverage can be increased by testing through these components using ScanExpressTPG.

❑ Connect all I/Os to boundary-scan controllable devices. This will enable the use of boundary-scan, digital I/O module, such as the ScanIO-300LV, to test all your I/O pins, thus increasing test coverage.

Summary

Boundary-scan is a widely practiced test methodology that is reducing costs, speeding development, and improving product quality for electronics manufacturers around the world. By relying on an industry standard, IEEE 1149.1, it is relatively quick, easy, and inexpensive to deploy a highly effective test procedure. Indeed, for many of today's PCBs, there is little alternative because of limited access to board-level circuitry. This paper highlights just some of the potential applications of the boundary-scan standard in various stages of the product life cycle, each contributing to the overall effect of significantly reduced product development and support costs.

References

The IEEE Std 1149.1-1990 - Test Access Port and Boundary-Scan Architecture, and the Std 1149.1-1994b - Supplement to IEEE Std 1149.1-1990, are available from the IEEE Inc., 345 East 47th Street, New York, NY 10017, USA, 1-800-678-IEEE (USA), 1-908-981-9667 (Outside of USA). You can also obtain a copy of the IEEE 1149.1 standard from http://www.ieee.com/

For more information about Corelis products and services, visit http://www.corelis.com

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